TECHNICAL MANUAL

No. 11-5805-786-12-1

HEADQUARTERS
DEPARTMENT OF THE ARMY
Washington, DC, 1 August 1997

OPERATOR'S AND UNIT MAINTENANCE MANUAL

COMMUNICATIONS CENTRAL AN/TTC-50

(NSN 5895-01-349-8064) (EIC: N/A)

REPORTING ERRORS AND RECOMMENDING IMPROVEMENTS

You can help improve this manual. If you find any mistakes, or if you know of a way to improve the procedures, please let us know. Mail your letter, DA Form 2028 (Recommended Changes to Publications and Blank Forms) or DA Form 2028-2 located in back of this manual direct to: Commander, US Army Communications-Electronics Command and Fort Monmouth, ATTN: AMSEL-LC-LEO-D-CS-CFO, Fort Monmouth, New Jersey 07703-5007. The fax number is 732-532-1413, DSN 992-1413. You may also e-mail your recommendations to AMSEL-LC-LEO-PUBS-CHGcecom3.monmouth.army.mil

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ENVIRONMENTAL REQUIREMENTS:

	Operation	Storage and Transit
Temperature	-40° F to 120° F (-40° C to 49° C)	-70° F to 160° F (-57° C to 71 ° C)
Altitude	Sea level to 10,000 feet (3,048 meters)	Sea level to 40,000 feet (12.192 meters)
Humidity	5% to 95% relative humidity	5% to 95% relative humidity

HCU:

SPARC20 cpu
3.5-inch floppy disk drive
2.1 GB removable hard disk drive (two)
Eight serial ports
SCSI port
12 MB RAM
1280 x 1024 pixel, 24-bit, 76 Hz video card

PERFORMANCE DATA:

Acoustical Noise — Less than 75 db (all equipment operating including ECU)

Signal Characteristics

Data rate	16 kb/s, 256 kb/s

POWER REQUIREMENTS:

Prime input power	115 Vac, 60 Hz, single phase
Alternate dc power	+28 Vdc
Emergency power	+24 Vdc

Section III. PRINCIPLES OF OPERATION

1-13 SYSTEM FUNCTIONAL DESCRIPTION.

1-13.1 Digital Switching. Digital switching is performed by hardware switching equipment located within the shelter TDSG (refer to fig. 1-4 and FO-1, TM 11-5805-786-12-3). This equipment lends itself to digital call processing, which provides the following:

- Circuit switch digital switching
- Line termination
- Signaling capability.

1-13.2 Routing. The routing function performs subscriber and network management. The subscriber features include the following:

- Preaffiliation of directory numbers
- Affiliation/reaffiliation
- Subscriber location
- Disaffiliation or absent service
- Blacklist management.

The network management features include the following:

- Call routing
- Duplication of subscriber directory
- Essential user bypass
- Automatic communications with the SCC.

The routing function provides the capability to find the called subscriber regardless of subscriber location, congested or blocked links, partial destruction, or equipment failures. This capability is performed by the flood search routing function (FSRF), which locates and marks a circuit path to the called subscriber.

A Data Terminal Adapter (DTA) is included within the routing function which provides an interface to the SCC through the network. It enables the SCC to access the TDSG of the CC shelter and to automatically update the switch database. It is also used to exchange operational messages between the Signal Commander at the SCC and the SCC terminal operator in the management shelter.

The routing function maintains lists of preaffiliated, affiliated, and duplicated subscribers, and manages the routing to subscribers and gateways. An interface to the routing function in the central processor is used for routing requests, man-machine requests, and the transmission of preaffiliated lists. The preaffiliated lists are read from the workstation load disk to the central processor routing function.

1-13.3 Control and Timing. The Master Timing Generator A (MTG A) is the source for the clock and timing signals needed to operate the TDSG. A backup, Master Timing Generator B (MTG B), is provided in case the primary MTG A becomes faulty. Both the primary MTG A and the backup MTG B are shown in figure 1-5. Each MTG consists of a precision voltage-controlled oscillator (MTG oscillator assembly), a controller (MTCTA), a synthesizer (MTGSY), and a distribution driver (MTGDR). Normally, primary MTG A is operating while backup MTG B is on standby, ready to take over if the primary MTG A fails.

The MTG oscillator assembly in each MTG is phase-locked to the reference oscillator (frequency standard). The controller circuit, together with the MTG oscillator, generate a 12.288-MHz square-wave signal. This signal goes to the synthesizer and is used to generate 18.432-MHz, 16.384-MHz square-wave signals, and 100 Hz sync pulses. These signals and sync pulses then go to the distribution driver where they are distributed to the digital line drivers in the TDSG.

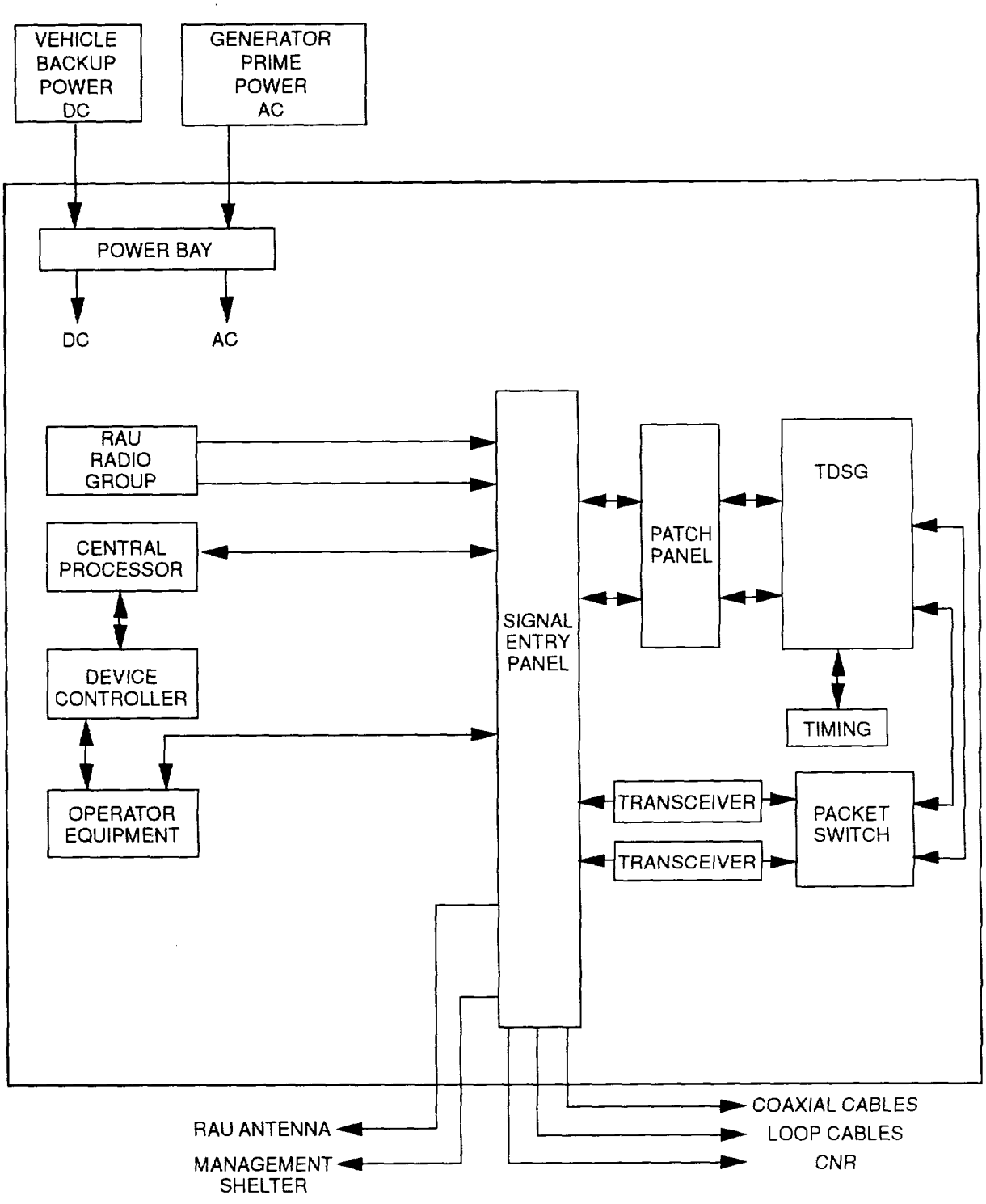

Figure 1-4. Circuit Switch Block Diagram

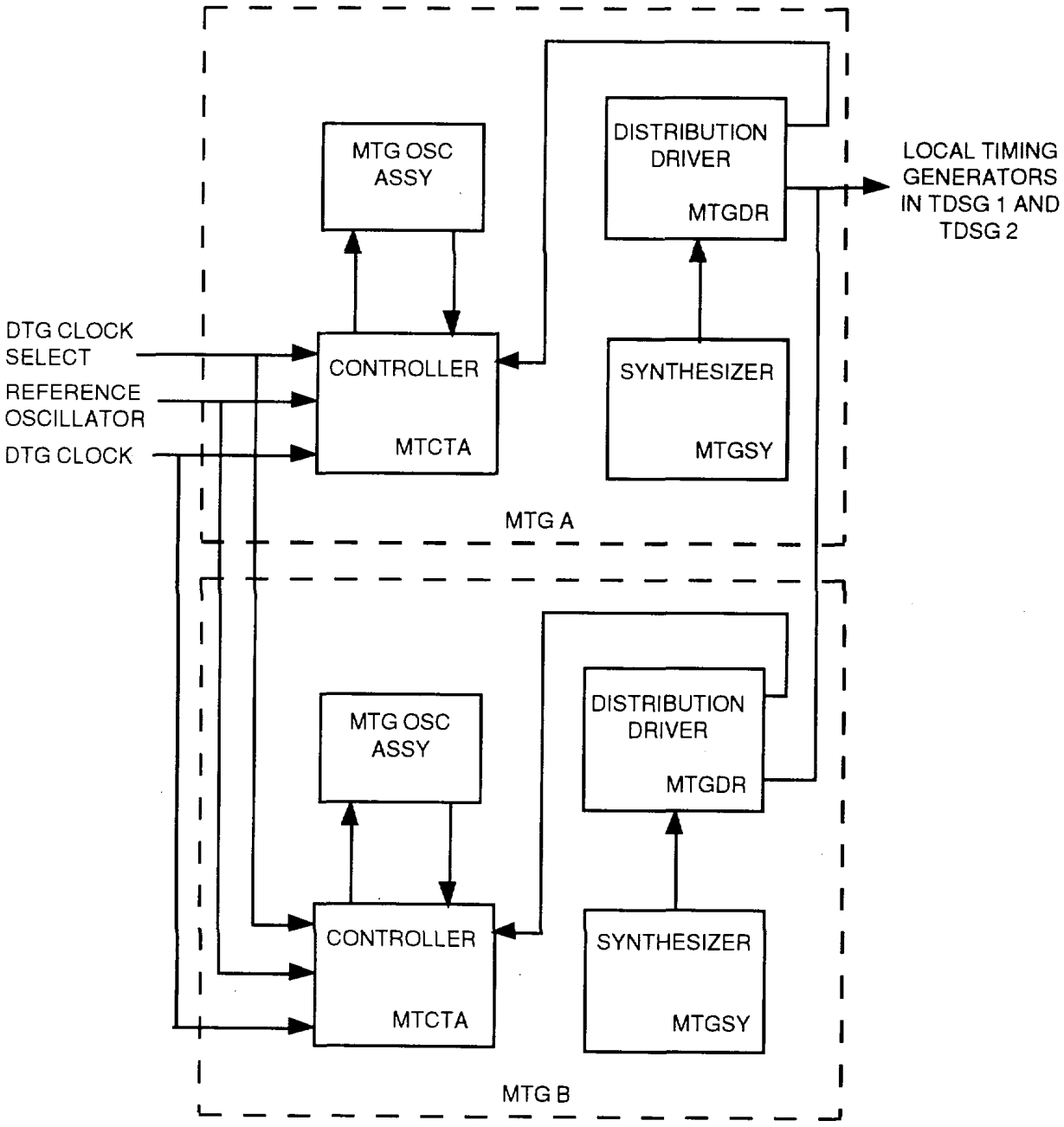

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Figure 1-5. Master Timing Generator Block Diagram

If the reference oscillator becomes faulty, provision is made to select the clock frequency on DTG 1 or DTG 16 as the MTG reference. Selection of the DTG is made by means of a switch on the patch panel. If the reference oscillator and the clock frequencies on the DTGs become faulty at the same time, the controller switches to internal reference control for stand-alone operation. If MTG A fails, MTG B is automatically switched on-line by the controller, and MTG A can be removed from the nest for repair without disturbing the operation of the nest.

1-13.4 Central Processor Group (CPG). The CPG is the link between software and hardware. It is an OL-386/TTC-39A processor used in an on-line standby or off-line configuration. The processor includes an arithmetic processor, an I/O exchange, microsequencer, front panel interface, micromemory, dual I/O exchange. and a solid-state memory unit. The CPG also includes the CPG controller group and two status and control panels. The prime functions of the CPG are call processing, flood search routing, and switch control. The software functions include start-up, recovery and interrupt control, on-line processing, fault detection, and diagnostics.

1-13.5 Power Group. The power group controls, distributes, and monitors the ac/dc voltages for the shelter. This group also provides voltage and power levels for the ECUs and housekeeping loads. The group includes the power entry and distribution control panels. It also includes the ac/dc regulators, batteries, battery charger, dc/ac converters, and power processor modules.

1-13.6 Personnel/Machine Interface. The personnel/machine interface is made up of hardware devices through which shelter operating personnel may communicate with the circuit switch. This interface group consists of the following:

- Shelter intercommunication facility
- Digital voice orderwire
- Workstation, consisting of:
  - Digital computer
  - Floppy drive
  - Visual display and keyboard
  - CSP headset control
  - Printer.

1-13.7 Circuit Switch Software. The circuit switch software monitors and controls the operation of the circuit switch. It provides the call processing software (of the digital switching capability) for the circuit switch.

The circuit switch software consists of a switch-subscriber database and a circuit switch on-line operations program (CSOLOP). The CSOLOP includes the person/machine interface and on-line fault detection programs. CSOLOP also includes the flood search routing function (FSRF) software.

The workstation is in the CC shelter and consists of the display, keyboard, digital computer, floppy drive, CSP headset control, and printer. It performs the following functions: provides assistance to subscribers, maintains a historical log file of switch activity, performs database updates, file maintenance, and the MTA/TNS MAINTENANCE function.

Each of the above tasks are performed using the display, keyboard, and specific software programs embedded within the WSOLOP.

1-13.8 Packet Switching Group (CC). The packet switching group provides the ANiTTC-50 with packet switching data communication capability. It also handles electronic mail for the associated packet network. The packet switching group consists of the following:

- Packet switch
- Transceivers (2)
- Host workstation
- Packet switch host/trunk interface (PSHTI).

1-14 NORMAL CALL SEQUENCE OF EVENTS.

The MSE network uses digital telephones almost exclusively. Analog interfaces can be accommodated using digital line termination cards (DLTUs) instead of the diphase loop modem at the switch or remotely in the CCV-4180(V).

The following paragraphs depict the normal sequence of events for completing a digital call between two local DNVT subscribers.

1-14.1 Request for Service. The following sequence of events takes place when subscriber B goes off-hook to initiate a call (fig. 1-6).

- Diphase Loop Modem A (DLPMA) cards are used as the line termination unit (LTU) for the DNVT
- Subscriber B goes off-hook. A seize codeword is sent to the circuit switch
- The seize codeword is detected by a digital scanner monitoring the assigned TDMX termination
- The switch sends an acknowledgment codeword from the DSG to subscriber B
- Dial tone is returned to subscriber B. The tone originates as a digital bit pattern which is sent from the digital signal generator (DSG) via the TDMX to the LTU.

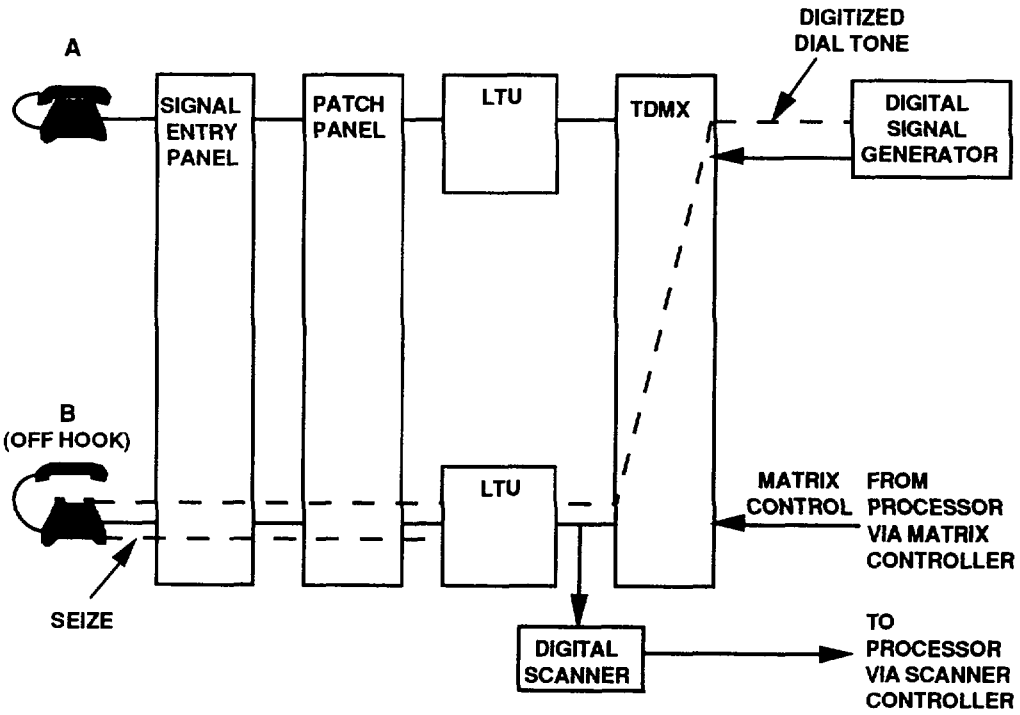

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Figure 1-6. Request for Service Block Diagram

1-14.2 Dialing Digits (Fig. 1-7). The following sequence of events takes place to process dialed digits:

- The processor assigns a digital receiver through a path to subscriber B
- Subscriber B, having received a dial tone, keys in the digits of the called party (subscriber A)
- Subscriber B sends the dialed digits to the switch as codewords. The digital codewords are sent to the digital receiver via the matrix (TDMX)
- The digital receiver reports reception of the first digit to the processor and discontinues the dial tone
- The switching function having received all of the digits, asks the routing function to find a route to the dialed subscriber. In this case the routing function reports that the subscriber is local. The switching function then attempts to ring subscriber A
- If subscriber A is busy, subscriber B receives a busy tone from the DSG
- If the call cannot be completed due to the lack of equipment, the out-of-service announcement will be generated by the interrupt recorder and sent to subscriber B via the DSG. If subscriber B attempts to make a call with a precedence above what is authorized, the precedence-violation announcement is sent, and the call is completed at the authorized precedence.

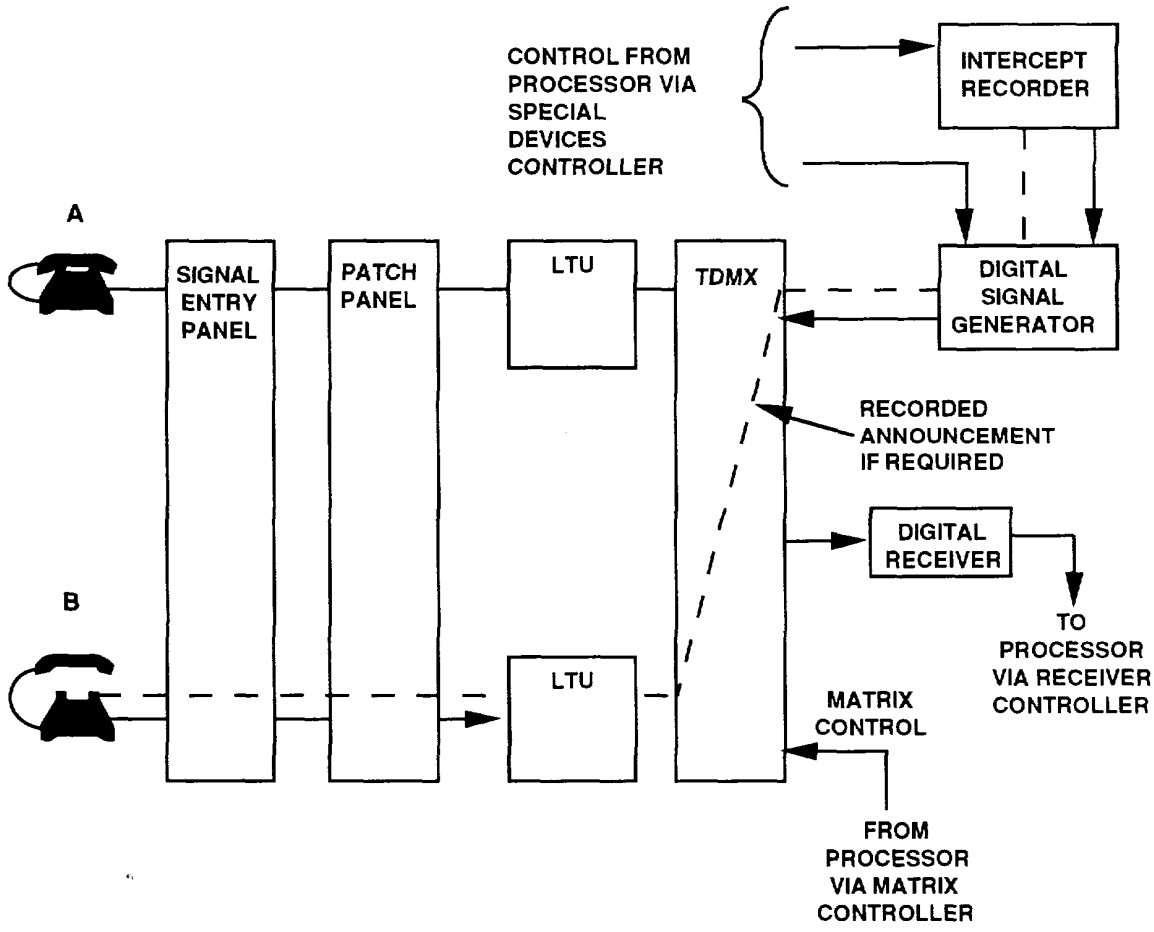

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Figure 1-7. Digit Receiving Block Diagram

1-14.3 Ring Phase. The TDMX connection to the digital receiver is removed and subscribers A and B are connected through the TDMX to the DSG. A ring voice (RV) codeword is sent via the LTU of subscriber A. The DNVT in turn generates the ring signal to the subscriber. Ring back is sent to subscriber B as a digital bit pattern from the DSG. It is converted to the audible ring-back tone by the CVSD in the phone (fig. 1-8).

1-14.4 Call Answer Phase. The following sequence of events takes place when a call is answered (fig. 1-9).

- Subscriber A goes off-hook and a seize signal is sent to the switching controller group where it is detected by the digital scanner.
- The seize codeword is acknowledged, and after additional handshaking the subscribers are connected through the matrix in the traffic mode.

1-14.5 Call Complete. When the subscribers are in traffic, the LTUs are connected through the matrix (TDMX). Analog voice signals are converted to a digital bit stream by the CVSD in the DNVT, sent through the digital matrix, and converted back to voice by the CVSD in the other DNVT (fig. 1-10).

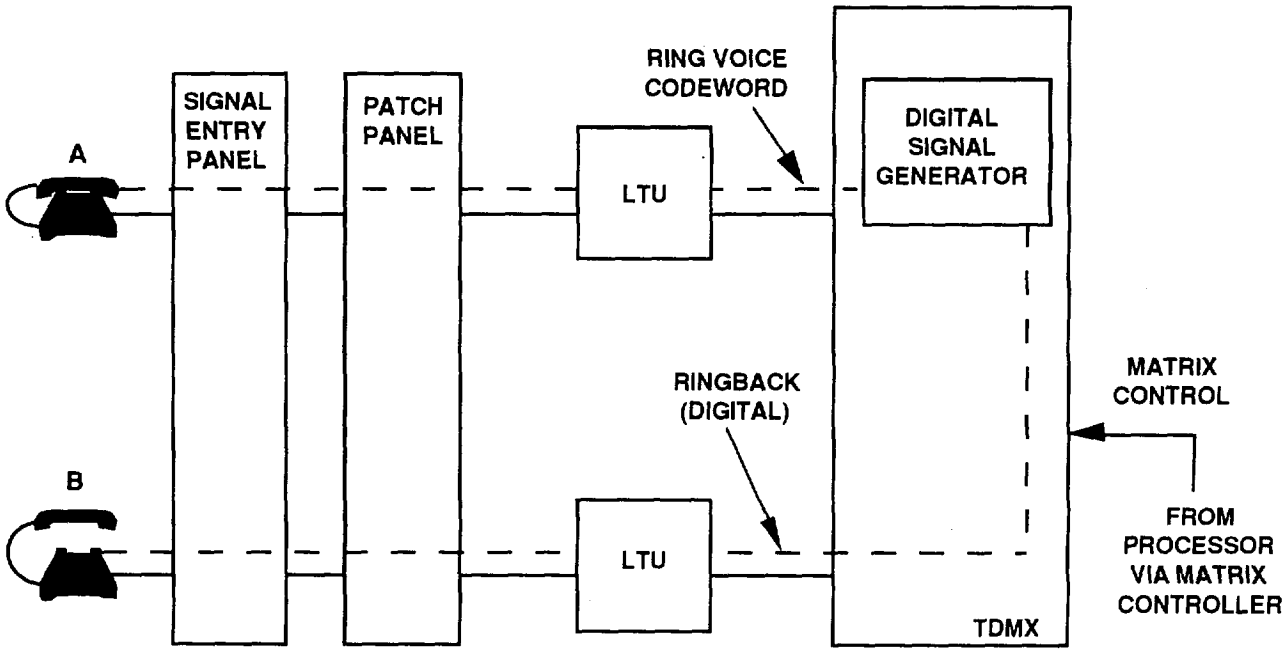

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Figure 1-8. Ringing Block Diagram

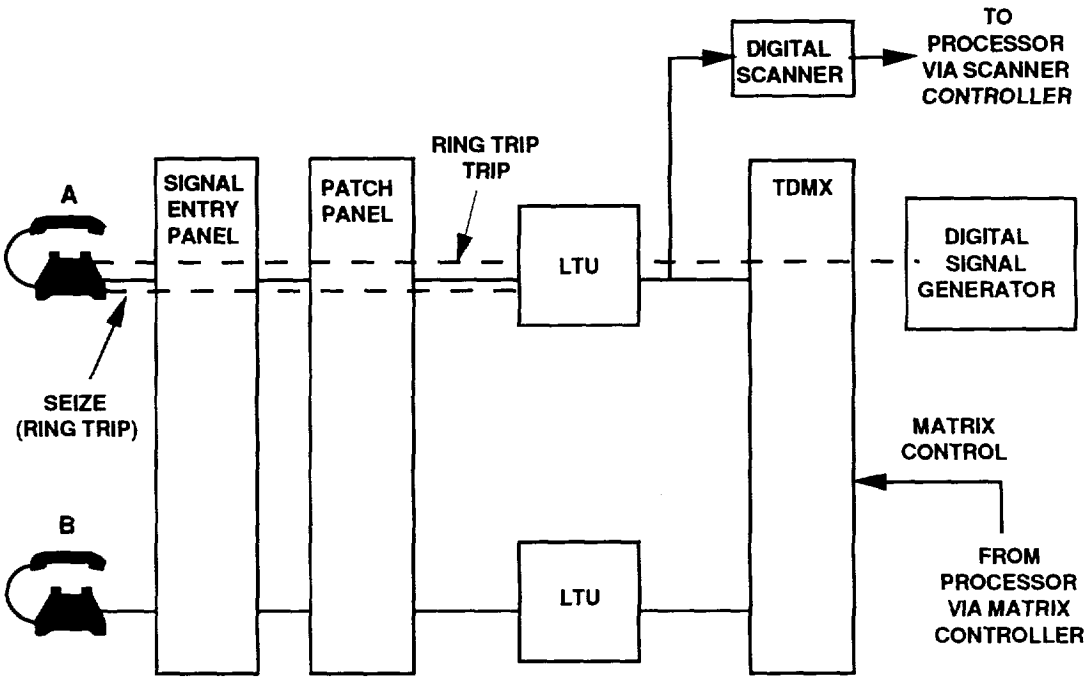

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Figure 1-9. Call Answer Block Diagram

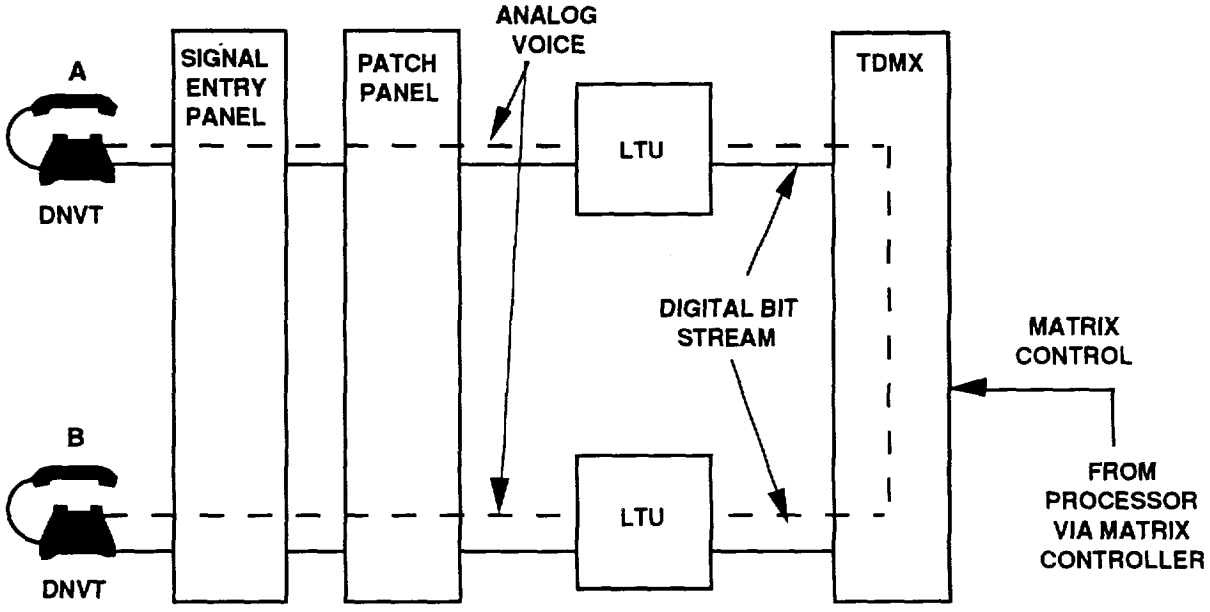

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Figure 1-10. Call Complete Block Diagram

1-14.6 Conference Call. The following sequence of events take place to make a (progressive) conference call (fig. 1-11).

- The originator goes off-hook, receives a dial tone, indicates precedence (if desired) then keys C to request a conference call. The processor checks the originator's class mark for conference privilege. If the originator is not class marked for conferring, an error tone is received by the originator
- If all conference bridge units are busy, the originator receives a busy tone. If a conference bridge unit is available, the originator receives a dial tone
- The originator keys the number of the first subscriber
- When the call is answered, the called subscriber and the originator are connected to the conference bridge unit through the TDMX and dedicated CVSDs
- After an answer is received, the originator may add other conferees by: keying C, wait for a dial tone, and proceed as in the preceding two steps.

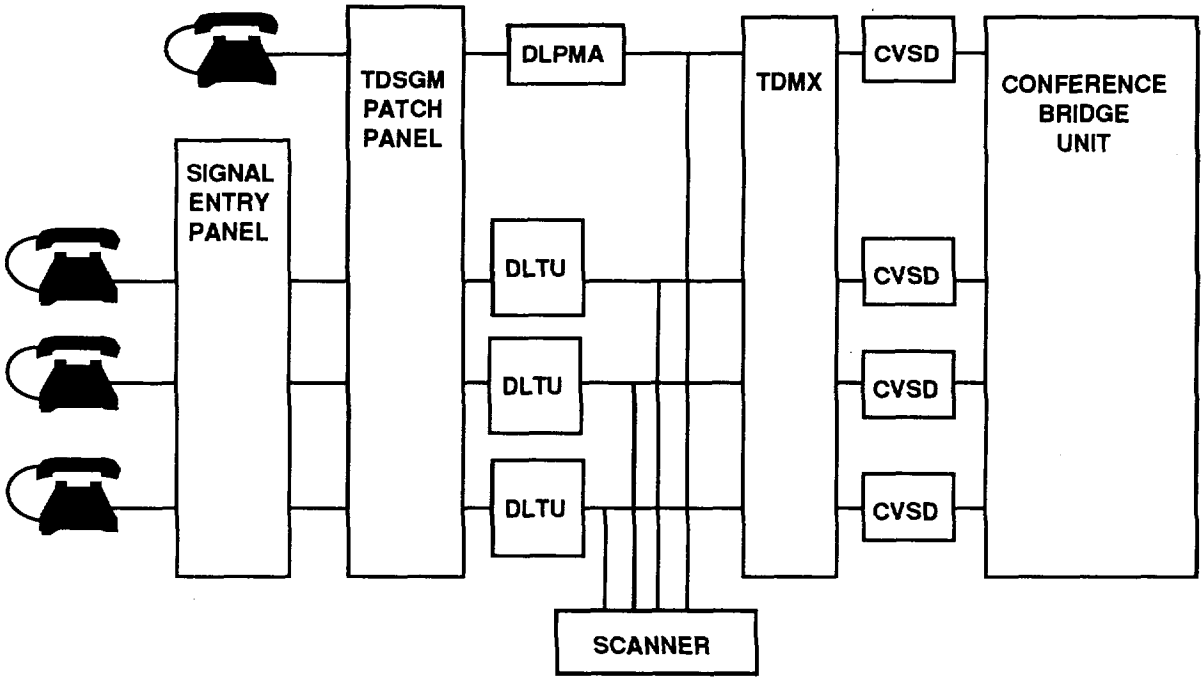

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Figure 1-11. Conference Call Block Diagram

1-14.7 Subscriber Release. When one of the subscribers goes on-hook, the subscriber sends a release to the circuit switch. The digital scanner detects the release codeword and reports it to the processor (fig. 1-12).

1-14.8 Call Release. When one of the subscribers goes on-hook (release), the release codeword is detected, the connection between the subscribers is broken, and a release acknowledge codeword is returned to the LTU. The on-hook telephone set and LTU return to the idle state (fig. 1-13). The DSG sends a digitized tone to the off-hook DNVT. The CVSD in the DNVT converts it to an audible tone. The subscriber hears the tone and goes on-hook. When the off-hook subscriber goes on-hook (release) the digital scanner detects the release codeword and the release acknowledge is returned from the DSG.

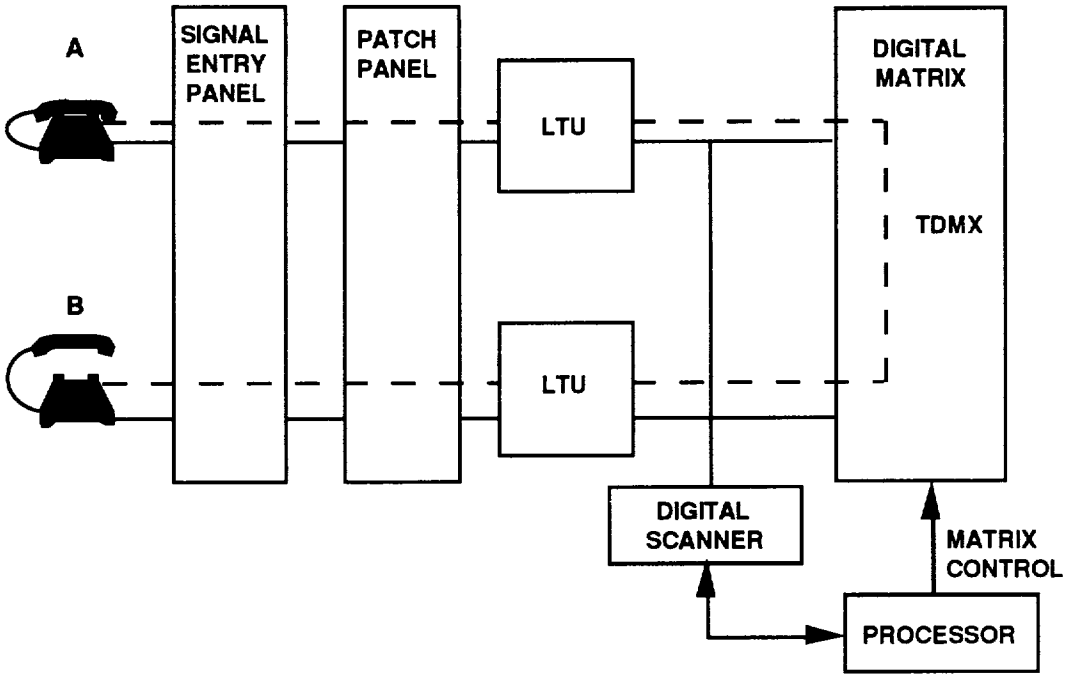

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Figure 1-12. Subscriber Release Block Diagram

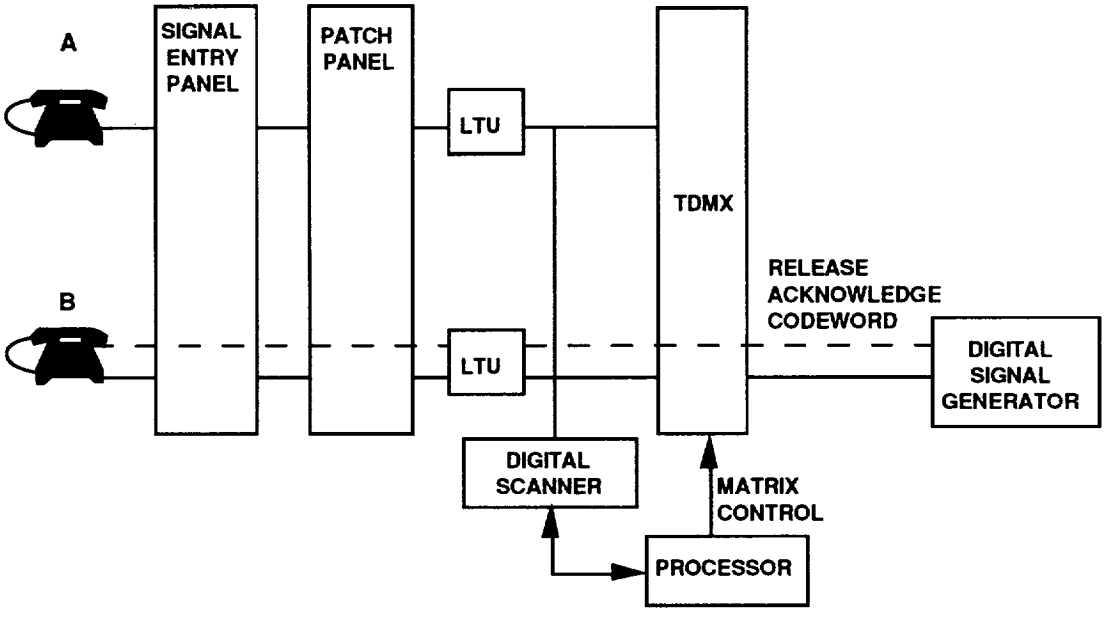

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Figure 1-13. Call Release Block Diagram

1-15 SIGNALING FUNCTIONS.

A summary of the codewords used for signaling between the CC switch and the digital phones and DLTUs is provided in table 1-3. Note that the codeword can have several meanings, depending on how it is used. All the listed codewords can be detected by digital receivers and DLTUs.

Table 1-3. Codewords

CODEWORD	SIGNAL NAME	ABBREVIATION	BIT PATTERN	DSG ADDRESS	TO SWITCH	FROM SWITCH
	Minor Channel Framing		1111 1111 0111 1111	00		
3	Digit 3, CUE X	D3 CUE	1111 1100	01	X	X
4	Release	RLSE	1111 1010	02	X	
5	Seize R KeyR	SZ X	1111 1010	03	X	X
6	Digit 7	D7	11101110	04	X	X
14	Digit 1	D1	1111 0000	05	X	X
15	Digit 4	D4	1110 1000	06	X	X
16	Digit 2 DSVT only Go Half/Duplex	D2 GHX	1110 0100	07	X	X
17	Priority Precedence Go Half/Duplex ACK (DSVT only)	P GHX-ACK	1110 0010	08	X	X
18	FKey Flash precedence Ring Data, ACK (DSVT only)	F RD,RIAD	11001100	09	X	 X
19 Force Clear	Digit 8	D8	1101 1000	10	X	X
20	I Key Immediate Precedence Ring Voice, ACK (DSVT only)	 RV, RIAV	1101 0010	11	X	
21	Flash Override Precedence Ring ACK Dial	FO RA DIAL	1101 0100	12	X X X	 X X
22	Digit 6 Release ACK Ring Trip	D6 RLSE ACK RT	1100 1010	13	X X	X X
23	Interdigit Idle	ID IDLE	1010 1010	14	X X	X X

Table 1-3. Codewords - Continued

CODEWORD	SIGNAL NAME	ABBREVIATION	BIT PATTERN	DSG ADDRESS	TO SWITCH	FROM SWITCH
31	C Key		1000 1000	15	X	
	Conference	C			X	
	End of Dial	EOD			X	
32	Digit 9	D9	1001 0000	16	X	X
	Go To Sync (DSVT only)	GTS				
33	Digit 0	D0	1010 0000	17	X	X
34	Digit 5	D5	1100 0000	18	X	X
	Go to Plain Text (DSVT Only) GPT			X		
36	Lockin	LI	0000 0000	19	X	
	Lockin ACK	LIA				
	Zeros					
1	Ones	ONES	1111 1111	22		
	Non-Secure Warning Tone (16 kHz)			26		
	Ring-back Tone (16 kHz)			29		
	Dial Tone (Normal)			30		
	Dial Tone (Call Transfer)			31		
	Line Busy Tone			32		
	Conference Disconnect Tone, Preempt Tone			34		
	N/A			37		
	Error Tone			38		
	Ring-back Tone			39		
	Ring Normal Tone			40		
	Ring Priority Tone			41		
	Seize Ack Tone, Release Ack Tone, Ring Trip Tone			42		
	Out-of-Service Recorded Announcement (Intercept Recorder)			44		
	Precedence Violation Recorded Announcement (Intercept Recorder)			45		
	Conference Notification Recorded Announcement (Intercept Recorder)			46		
	Conference Notification Recorded Announcement From Recorder			47		
	TDMX Misrouting Test			48		
	Zone Restriction Recorded Message			49		
	DSG Test Tone (571 Hz Continuous + 8db For Pre Ring Tone Test)			50		
	CVSD Test Tone for Half Rate (16 kHz) Setting (500 Hz Continuous -10db)			51		
				52		

1-16 DIGITAL SWITCHING, MAJOR FUNCTIONS.

1-16.1 General. Digital switching is performed by hardware elements that lend themselves to the digital call processing function (refer to FO-1, TM 11-5805-786-12-3). These hardware elements provide an interface with up to 164 digital subscribers, 24 using junction boxes and 140 via four dismounted LTUs, CV-4180. The CC standard database uses one 32-channel digital trunk group for connecting to an NC switch (refer to fig. 1-14). The database also allows a 72-channel TACSAT DTG to an NC (refer to fig. 1-15). There are also provisions for DTGs to two RAU and two SEN switches. The SEN used with the CC is normally the Communications Switching Set (CSS) AN/TTC-51.

Encryption of DTGs is provided by a trunk encryption device (TED). It is placed in series with the transmission path.

Loop encryption is provided by a loop key generator (LKG) selected from the COMSEC equipment facility and switched through the matrix to service a particular digital loop.

On DSVT calls link encryption is provided by encryption built into the phone. LKGs are used for call set up. All incoming signals are converted to 16-kb pulse rate for digital processing. The 16-kb train is switched through a multistage multiplexing and demultiplexing (mux/demux) chain. This serial pulse train is routed to the TDMX, which provides switching by transposing the time-ordered bit location (subscriber lines) of the outgoing pulse train.

The primary mode of transmission for digital loops and digital transmission groups is diphase modulation. Conditioned diphase modulation is employed for transmission over wire and cable.

Interswitch DTGs used for the links to NC switches employ a method called common channel signaling. Within each digital trunk group, a portion of one channel is used to carry the signaling and supervisory information for all trunk group subscribers.

The circuit switch uses a common 16-kb digital signal channel. Multiplexing is performed internally to the circuit switch, then transmitted to the distant switch.

System timing is derived from the frequency reference oscillator (FRO) or incoming synchronous bit pattern. This bit pattern (recovered clock) is extracted by the group modem and sent to the circuit switch MTG, from the selected DTG (DTG 1 or DTG 16).

In addition to trunk group signaling information, the common channel writes timing information (framing). The framing pattern is used to identify the channels in the bit stream. A second channel is used for flood search routing.

1-16.2 Digital Inputting. Digital switching inputs for digital loops are made with 12-pair (4-wire) subscriber cable (red or black). Individual coaxial pairs are used for transmission groups.

Local subscriber groups are connected to the CC in groups of 12 via 26-pair cables which are connected to a junction box external to the switch. The junction box is cable connected to one of two connectors on the SEP. Inside the CC the input is connected to LTUs in the TDSG. The transmit and receive pairs are routed via normally through connection of the patch panel. The CC is populated with six diphase loop modem (DLPMA) cards for interfacing up to 24 DNVT or DSVT digital phones. DLTUs may be substituted to interface with analog subscribers, which may be analog phone or trunks. The DLPMA cards convert the conditioned diphase signaling from the phone to baseband digital, which is input to a time division memory module (TDMM) of the digital matrix through the loop mux/demux to a switch mux/demux and nine channel muxes (p/o group mux/demux).

Eight DTGs are connected to coaxial connectors at the CC switch SEP. The DTGs are routed to coax connectors on the patch panel and then manually patched to a group modem (GM). The GM converts the multiplexed signals from baseband to diphase (or dipulse) signals. This data is then input to the group buffer in the TGM. The TGM is a first in/first out (FIFO) buffer providing timing elasticity (bit breathing) to compensate for timing source variations between local and remote switches. Normally, timing comes from the reference oscillator but may come from a recovered clock from DTG 1 or DTG 16, as selected at the patch panel. Data is forwarded to the group framing unit (GFU) in the TGM where frame channel identification and alignment is performed. On

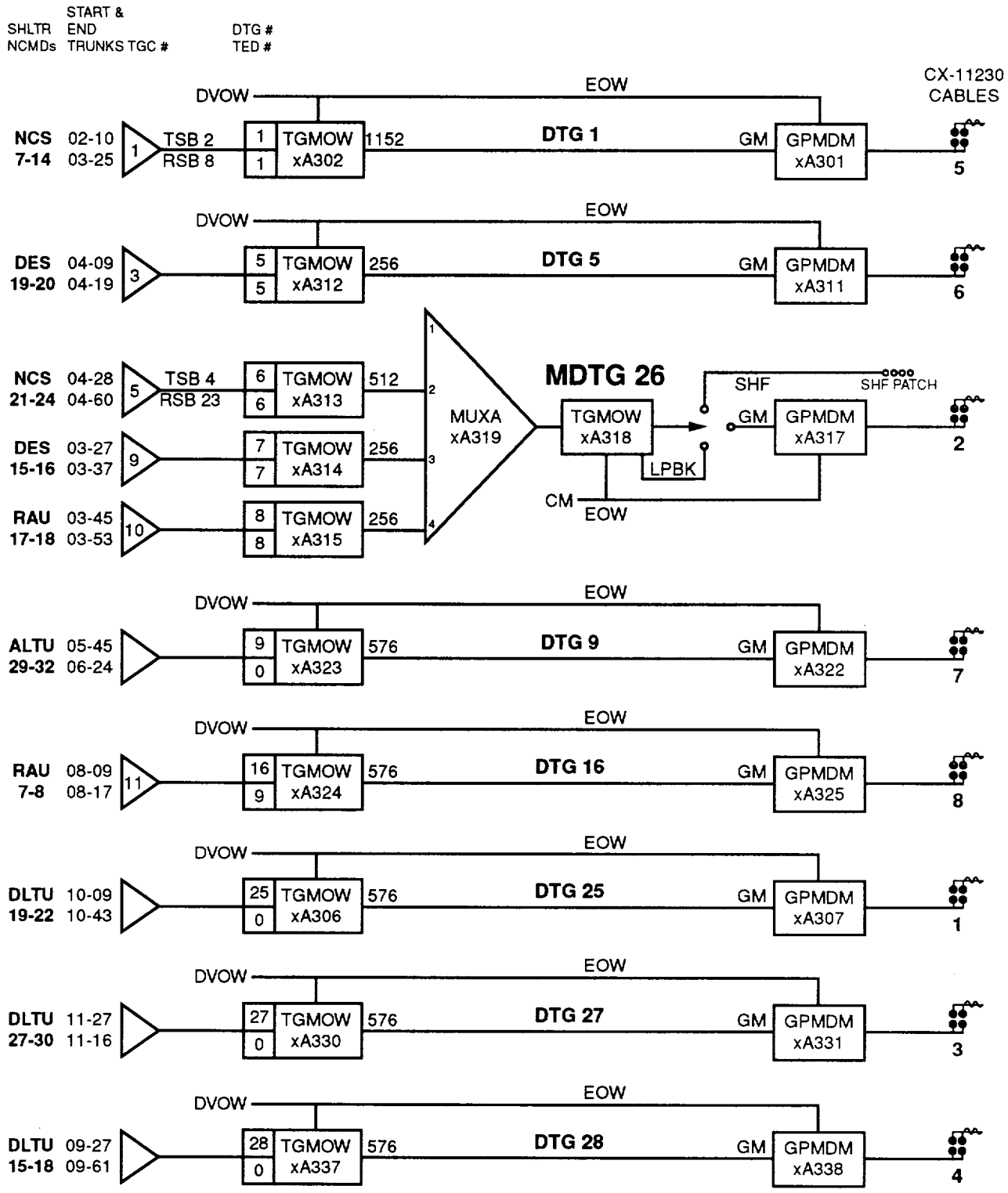

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Figure 1-14. CC Standard Database Configuration

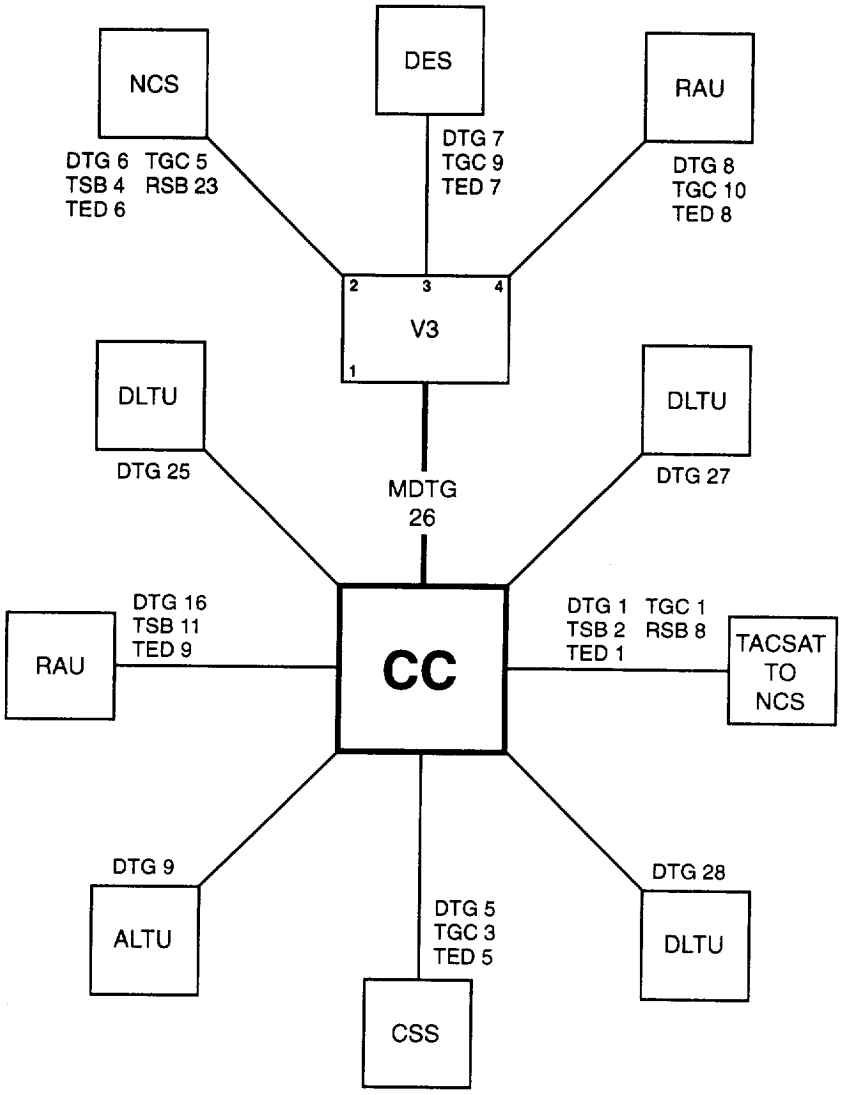

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Figure 1-15. CC Standard Database Assignments

interswitch links a TED is added between the group buffer and the GFU. DTG 26 is a multiplexed DTG (MDTG). Three separate DTGs are multiplexed into a single bit stream.

Automatic hardware synchronization is provided for frame synchronization of the TGM.

The outputs of the GFUs are time synchronized and simultaneously input to the group mux/demux. The mux/demux unit consists of two chains of 36 nine-channel multiplexers and demultiplexers (NCMD). The 324 channels of each NCMD chain are wired to dedicated terminals on the time division switching matrix. The DTG channels are connected through the matrix to 648 16-kb lines. These are combined with the service and test terminals in the switch multiplexer and demultiplexer.

The standard CC database has one 32-channel DTG and one 72-channel DTG to NC switches. The 72-channel DTG is via TACSAT. There are also two 16-channel DTGs to DES switches and two 16-channel DTGs to RAU switches. The standard database also has four DTGs that connect to remote wire subscribers via the LTU CV-4180(V), a remote module that can terminate up to 35 single-channel analog or digital loops, or analog trunks. Each switch multiplexer and demultiplexer interfaces 64-channel time multiplexed pulse trains to the TDMX for switching.

Digital switching involves the transportation of incoming and outgoing lines in a random access memory (RAM).

1-16.3 Scanning. The CC has four digital scanners. Each scanner scans the terminals on three TDMMs (192 terminations). Only TDMMs 1 through 12 are scanned. The scanner detects eight specific codewords.

Scanning incoming digital lines is performed at the output of the switch multiplexer and demultiplexer. When the digital scanner detects a request for service, the request is sent to the processor through the scanner controller. The processor then steps through a series of call processing software routines to select and guide the hardware through the call connection process.

1-16.4 Digital Signaling and Supervision. The full range of circuit switch services and switching functions are available to all digital subscribers (DNVT and DSVT subsets) and to a limited degree to analog subscribers which home in on the TDMX switch through DLTUs.

The major control operations involved in providing these services are primarily related to the supervision, information or address signaling, and the matrix connection for each call processed. The following paragraphs describe a call sequence using a COMSEC DSVT subset.

1-16.5 Call Process Sequence of Events.

1-16.5.1 Request for Service. When a call is initiated by a subscriber on loop no. 1, the digital scanner, which sequentially samples each incoming line, detects the demodulated seize codeword and notifies the processor that a service request (seize signal) has been detected on loop no. 1. The processor determines the type of subset used by the calling subscriber and connects the LKG crypto unit and digital receiver in preparation for the subscriber dial phase.

To notify the calling subscriber to initiate the dial sequence, the dial codeword and digitized tone signals are sent to the calling subscriber after connections from the DSG to the called subscriber are made.

1-16.5.2 Dialing Phase. The calling subscriber hears the dial tone, and keys in the called subscribers digits along with any applicable precedence digits and access codes. The keyed digits are detected at the switch by a digital receiver and forwarded to the processor. Receipt of the first digit causes the dial tone to be replaced with a send "ONEs" codeword generated by the DSG.

Upon receipt of the last digit, the switch signals the DSVT from the digital generator, to determine the mode (voice or data) of the subscriber, if the subscriber is class marked as a dual mode. The response to the signal (indicating voice or data mode) is detected by the digital receiver.

The digital receiver is then disconnected and returned to the pool by the processor. If the called subscriber is busy, a busy tone is connected to the crypto loop from the DSG. If the called subscriber is incompatible with respect to mode (voice or data), an error tone is sent to the calling subscriber.

1-16.5.3 Ringing Phase. If the called subscriber is compatible and non-busy, a compatible LKG crypto unit is connected to the called subscriber's DSVTs diphase loop modem, and a ring voice or ring data codeword is sent from the DSG.

The DSVT responds to the ring voice signal by activating its ringer and sends a ring acknowledge signal back to the switch. It responds to the ring data signal by electrically going off-hook and sends a ring trip codeword back to the switch. The switch detects ring acknowledge or ring trip with its digital scanner and responds by sending go to sync codeword or go to plain text, depending on the encryption mode of the call, to the calling party from the DSG.

The calling DSVT responds to these codewords by starting its internal ring-back tone generator and sending the lock-in codeword to the switch. The switch detects lock-in codewords with its digital scanner and responds by sending "ONEs" codewords from the DSG.

If the above is to be an end-to-end crypto connection, the calling DSVT no longer requires the LKG and it is disconnected and returned to the pool.

1-16.5.4 Ring Answer Phase. When the called DSVT goes off-hook, it sends a ring trip codeword to the switch. The switch detects ring trip with the digital scanner and responds by sending go to sync codewords or go to plain text, depending on the encryption mode of the call to the called DSVT from the digital generator.

1-16.5.5 Traffic Phase. When the switch has detected lock-in from both the calling and called parties, it returns LIA and then completes a connection between the calling and called party's diphase loop modems (end-to-end connections) or between the clear text sides of their LKG devices (link-by-link connections). Further codeword exchanges take place at this point between the two DSVTs. The switch processor ignores scanner reports of all further codewords except release and C key.

1-16.5.6 Conferencing. Digital subscribers are provided the conferencing (more-than-two-party call) privilege by connecting them through CVSDs to the analog conference bridge units (CBUs). Signal for such calls is the same as described for digital-analog calls (fig. 1-16).

1-16.5.7 Subscriber Release. When a DSVT goes on-hook, release codewords are sent to the switch. The switch receives the codewords through its digital scanner and responds by sending release ACK followed by a ONEs codeword (having disconnected the subscriber's diphase loop modem) to the DSVT.

A DSVT sending a release codeword will power down on receipt of a ONEs codeword. The switch processor also causes the LKG to be disconnected and returned to the pool.

1-16.5.8 Call Release. When a called subscriber connected to a DSVT subscriber releases, the switch signal sends a ONEs codeword from the DSG and disconnects the LKG and returns it to the pool. The DSVT subscriber hears silence and goes on-hook, which sends a release codeword to the switch.

The subscriber release procedure is followed from this point. The switch is capable of forcing digital telephones to go electrically on-hook which sends a release. This is done by sending cue and force clear codewords to the digital telephone from the circuit switch.

1-17 CONTROL AND TIMING, MAJOR FUNCTIONS.

1-17.1 General. The control and timing equipment is located in the common equipment group (CEG) within the TDSG (fig. 1-17). The control and timing equipment provides control and signaling which, when used with the digital switching group, provides facilities for the switching supervision and signaling of digital loops and trunks. The special devices controller provides the data path for the routing of signals and controls between the CPG

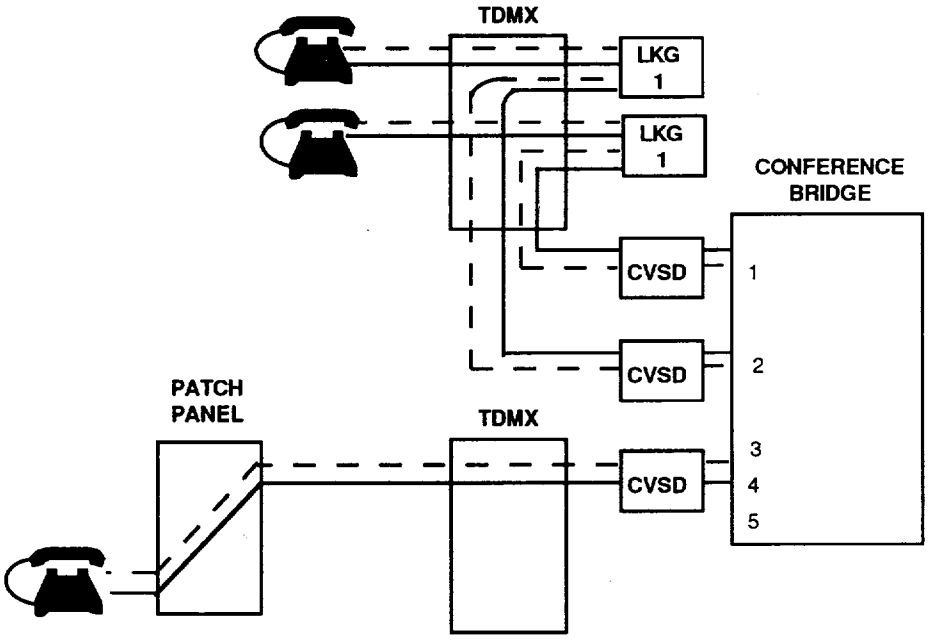

Figure 1-16. Conferencing Block Diagram

and a large number of miscellaneous devices. The matrix controller consists of two device controllers, one to send data to the time division matrix, and another to receive status data from the time division matrix.

Overall control of the circuit switch is exercised by the CPG through the SCG, signal buffer controller (SBC) and COMSEC controller (CC).

The SCG consists of the CPU central controller, the receiver controller, the fault controller, the scanner controller, the matrix controller, and the special devices controller. System timing is provided by the frequency reference oscillator, MTG and local timing generator (LTG). Configuration control and system fault display is provided by the control and alarm panel (CAP)/EOW control module.

1-17.2 Switching Controller Group. The SCG provides control of the circuit switch system by connecting the CPG with the digital switching group. The SCG provides the only system path for the routing of controls and data between the CPG and the digital switching group. The SCG consists of several individual device controllers. Each device controller interfaces with a specific set of devices requiring access to and from the CPG.

All device controllers interface with a single controller (CPU central controller). Its function is to provide an interface to and from the CPG and to control overall operation of the SCG. The scanner controller receives data from the digital scanners and reformats the data to proper form before sending it to the CPG. The receiver controller receives data from the digital receiver and reformats the data to proper form before routing it to the CPG.

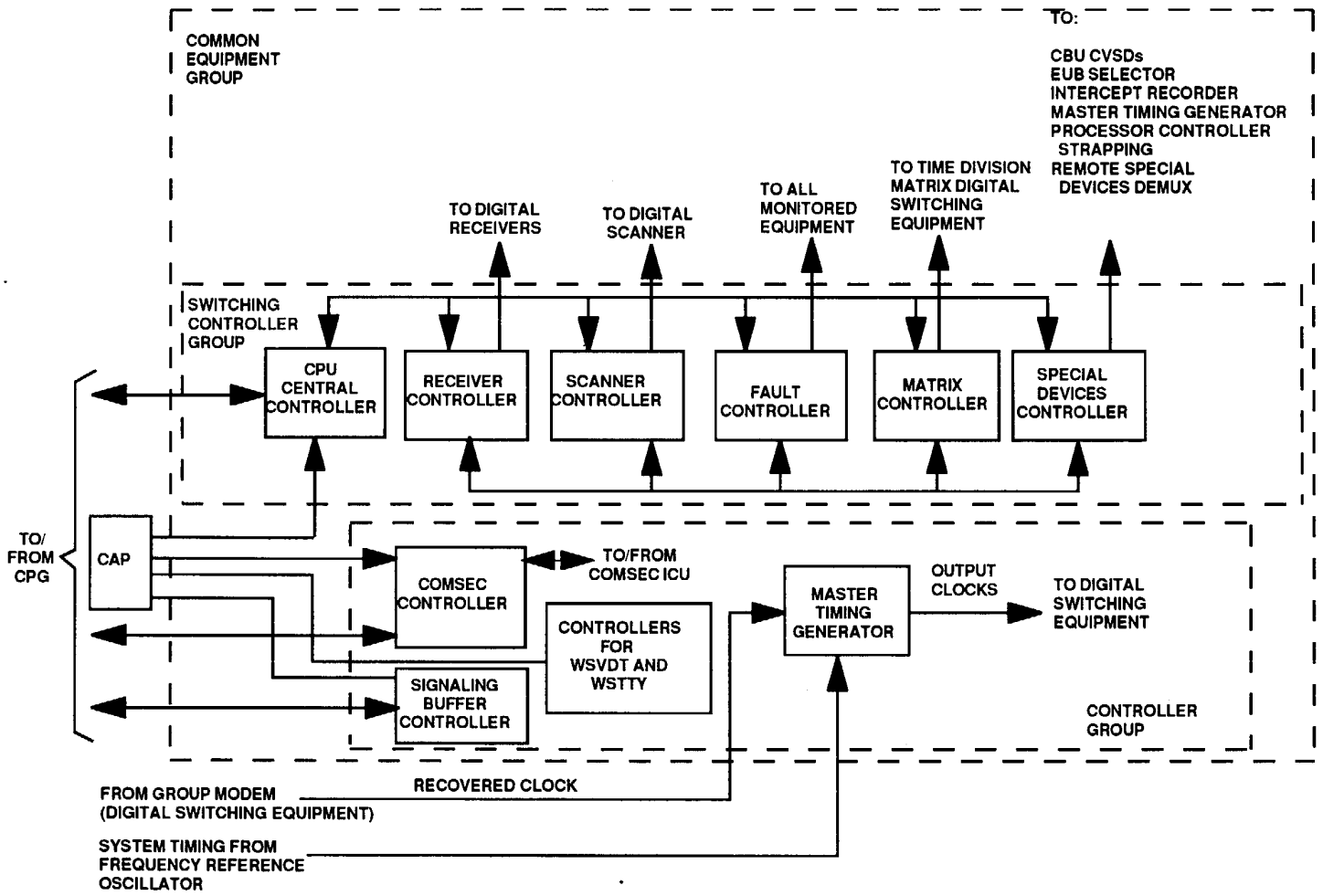

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Figure 1-17. Control and Timing Block Diagram

The fault controller sequentially scans all devices in the system, reporting faults and status. The fault controller compares the data obtained on the previous scan and, in the event of any change, reports the current information together with the device address to the CPG.

1-17.3 COMSEC Controller. The COMSEC controller connects the CPG to the COMSEC equipment. It provides bi-directional serial/parallel data conversions.

1-17.4 Signaling Buffer Controller. The signaling buffer controller interfaces the trunk signaling buffers, the remote SBC mux/demux (digital switching equipment), and the CPG. In addition, data from each buffer is formatted for transfer to the CPG.

1-17.5 Master Timing Generator. The MTG, along with the frequency reference oscillator (FRO) and local timing generator, provides all the clock signals required to operate the circuit switch.

The clock signals are normally generated by phase locking the MTG oscillator to the FRO.

The clock signals can also be synchronized with one of the two recovered clock signals.

1-17.6 Control /Alarm Panel. The CAP allows the operator to perform a number of functions and indicates a shelter fault to the operator by a simultaneous visual and audible alarm. A call processing initiate control on the CAP is used by the operator during system start-up to activate the central processor so that it begins processing on-line calls. The activating signal from the CAP goes to the central processor through the CAP interface panel and the device controller. EUB is initiated by the operator at the CAP. The initiating signal goes through the CAP interface panel and the signal entry panel to the switching shelter where the EUB switch connections are made. When the connections are completed, a signal is sent back to the CAP where it turns on a lamp indicating the connections were completed.

The CAP HANDSET SOURCE SELECT switch permits the operator to select either the operations shelter or the management shelter KY-57 handset. When the operations shelter handset is selected, the handset plugged into the CAP is connected to the KY-57 unit in the operations shelter through the CAP interface. When the handset in the management shelter is selected, the data from the handset in the management shelter enters the operations shelter through the signal entry panel and is connected to the KY-57 unit through the CAP interface panel.

The central processor serves as the functional interface between the operator equipment group and TDSG controller group to enable the performance of all call processing, flood search routing functions (FSRF), and switch control functions (including such features as progressive and preprogrammed conference calls, compressed dialing, call forwarding, and automatic line hunting). Database organization within the central processor allows for on-line integrated BIT monitoring of the central processor group through the display monitor.

The CPU provides the logic and computational capability to perform data comparison, data interpretation, status assessment, table search and arithmetic operations. It processes data collected by the IOU. Data is transferred in a 36-bit parallel format (includes four parity bits) between the CPU-IOU.

All data transfers between the central processor, the CPU controller (which services the circuit switch operating equipment) and the CPG peripherals occur over I/O channels and are serviced by the I/O controller within the IOU. The processor interface control unit serves the processor, providing the processor-to-processor data interface and access to the workstation.

The circuit switch central processor operates under software (stored program) control. The circuit switch programs reside in memory on the workstation hard drive (load disk). A description of the circuit switch software is provided in paragraphs 1-38 through 1-41. Input power is supplied to the CPG equipment by CPG power supplies.

1-18 POWER GROUP, MAJOR FUNCTIONS.

Refer to figures 1-31 and 1-32 for power group major functions. The power group includes the following:

- Cabling
- Power line protection
- Electromagnetic Interference (EMI) protection
- Power line current and voltage protection
- Internal shelter voltage distribution of all ac and dc requirements for the circuit switch.

The power is supplied for critical loads by an uninterruptible power subsystem. The subsystem derives a continuous power source from the prime power and battery backup system.

1-18.1 Power Entry Panel (PEP). The PEP is mounted on the shelter exterior wall. All panel connectors are waterproofed and a hinged cover provides protection against the environment. The PEP provides power receptacles for 60-Hz prime power cables. Circuit breakers are provided for the ECU. ESAs, EMI power line filters, and a ground stud are included as part of the PEP.

1-18.2 AC/DC Power Control Panel (AC Section). AC power is distributed via the ac/dc power control panel. Power to ac loads is distributed through circuit breakers on the panel. The circuit breakers provide load switching and overload protection. Each circuit breaker is labeled according to the load it controls. The ac section of the power control panel includes:

- Voltage, current, and frequency monitoring meters
- Phase rotation indicators for 60 Hz
- Audible alarm to indicate incorrect phase
- Blocking relay to activate main circuit breaker trip coil if incorrect phase rotation is present.

The non-critical ac loads are those that do not operate from the uninterruptible power system which relies on battery bank backup. These loads are not driven during the loss of prime ac input power to conserve the ampere-hour rating of the battery bank.

1-18.3 Regulator/Battery Charger. Regulator Portion. The regulator provides a dc source voltage from which secondary ac and dc voltages are derived. It accepts single-phase, 120 Vac, 60 Hz input power. The output voltage is +26.5 Vdc + 1%.

1-18.4 Regulator/Battery Charger. Battery Charger Portion. The battery charger is capable of recharging the bank of lead-acid batteries to 90 percent of capacity within 24 hours. The charger has a separate control to allow charging during the time the main power bus is not operating.

The battery charger voltage and state of charge may be monitored via meters provided on the ac/dc power distribution panel. Battery equalization charge time may be monitored via the elapsed time meter.

1-18.5 AC/DC Power Control Panel (DC Section). DC power is distributed via the ac/dc power control panel. The panel provides:

- DC voltmeter
- DC ammeter
- DC circuit breakers.

These instruments and switches service both the main branches and individual pieces of equipment. Controls and indicators for the battery charger are provided on the panel.

The panel circuit breakers are two-pole and are manually actuated as start or stop switches. Indicator lights show the status of all the individual dc loads. The emergency light switch is operated either from the dc power control panel or from a separate switch located near the door. Power to the dc loads is distributed through circuit breakers which are labeled to indicate the particular loads they control. The circuit breakers are employed to load switching and overload protection.

1-18.6 Batteries. The battery bank consists of two 6-TN lead-acid batteries that provide 10 minutes of emergency power.

The batteries are rechargeable and have a long life. They operate at low temperatures and are readily available. The 6-TN battery is rated at 12 Volts and 70 ampere hours at a 5-hour discharge rate. The battery box is vented to the outside of the shelter in order to remove hydrogen gas which is generated during the recharging cycle.

1-18.7 Power Processors. Power processors provide the secondary sources of dc power for those loads which require dc voltages other than that supplied by the dc bus. They have an input capability of 120 Vac at 60 Hz, or 26.5 Vdc.

The input circuitry of the power processors is such that a precedence technique is employed in the selection of the input voltage. The precedence is such that the prime ac voltage, when present in the shelter, is employed in powering the power processors. In the absence of prime ac power, or during degradation of this input source, the power processors automatically switch to the 26.5 Vdc main bus without degradation of the regulated output voltages.

1-19 PERSONNEL/MACHINE INTERFACE, MAJOR FUNCTIONS.

The personnel/machine interface consists of:

- Shelter intercommunication facility
- Workstation, consisting of:
  - Digital computer
  - Floppy drive
  - Visual display and keyboard
  - CSP headset control
  - Printer
- Digital voice orderwire.

1-19.1 Intercom. There is one intercom in each shelter. The voice signal from the intercom goes through the CAP interface panel and out the signal entry panel. The intercoms provide the operator with two-way audio communications between the CC shelter, and management shelter using the intershelter cables. In addition, this two-way audio communication can be extended to other switching, operations, and management shelters in the MSE network. This is done by patching the intercom jacks in the switching shelter patch panel to available cable jacks on the same panel. This makes connection to the shelter intercoms possible at the external J-1 077 junction box terminals associated with the cable patch panel jacks.

1-19.2 Workstation. The workstation (WS) consists of the display, keyboard, digital computer, floppy drive. CSP headset control, and printer. It performs six main switch functions: (1) provides assistance to subscribers: (2) maintains a historical log file of switch activity; (3) performs database updates; (4) performs file maintenance; (5) maintains the tactical name server and mail transfer agent functions; and (6) provides network services. Each task is performed using the display, keyboard, and specific software programs embedded within the WSOLOP.

1-19.3 Digital Computer. Digital computer (AN/UYK-86(V)3) provides for an external disk drive and two internally-mounted plug-in hard disk drives; the system disk drive and the load disk drive. The system disk drive contains the operating system and/or database program for the digital computer. The load disk drive contains the operating system and database programs for the switching processor unit (SPU). The external disk drive is used to download the operating system and/or database program software upgrade onto either the system disk drive (for the digital computer) or the load disk drive (for the SPU). An I/O to SCSI link (IOSL) CCA in an external controller nest facilitates the interface between the load disk drive in the digital computer AN/UYK-86(V)3 and the SPU.

1-19.4 Display Terminal and Keyboard. When the operator uses the display terminal and keyboard, communications with the central processor through the WS digital computer is established. Communication between WS and central processor occurs by means of two serial RS-232 interfaces. Signal routing is from the WS to the central processor through the VDT and TTY controllers. Three types of messages are sent between the central processor and WS over one of the serial interfaces: (1) messages for Call Service Position (CSP) control; (2) central processor status messages to the WS; and (3) operator-generated TTY mode messages to the central processor. The second interface is used to send/receive switch man-machine (MAMA) screens between the two processors.

1-19.5 Call Service Position. CSP is used to provide subscriber assistance. When a call is placed to the CSP, the subscriber is connected to the CSP bridge TDSG. Call service is performed as a software operation that is accessed through the workstation display terminal and keyboard. The CSP operator communicates with the subscriber using the CSP headset connected to the CAP/EOW control panel.

The CSP enables the attendant to assist the subscribers in the following categories:

- Local call completion assistance
- Directory and routing information
- Trouble reporting
- Trunk call completion assistance
- Busy and no answer verification
- Establishing conference calls
- Verbal precedence/preemption requests
- Call holding
  - Call splitting
- Establishment of secure calls.

1-19.6 Digital Voice Orderwire (DVOW). The DVOW is an EOW unit used in multichannel communications systems to provide digital voice communications between the local CC and remote shelters. The DVOWA and DVBRG cards in the TDSG modulate a DVOW channel onto any one of the DTGs that go out of the switching shelter over coaxial cables. The voice signal from the handset is encrypted by the KY-57 unit before going to the OCU/communication modem. The encrypted digital voice signal from the OCU/communication modem then goes to the EOW patch panel. From the EOW patch panel, the signal goes through the signal entry panel over one of the DVOW channels to the transmission group module orderwire (TGMOW) circuit card.

1-19.7 Workstation Printer. The workstation printer communicates with the WS by means of an RS-232 interface. The printer supports printing generated locally by the WS, and status messages received from the central processor over the serial interface. The printer is functionally shared by two WS processes. One process is the WS print queue. Printing requests generated by the operator are sent to the WS print queue and in turn are output to the printer. Switch status messages received from the central processor over the serial interface are buffered by the second process. Messages are then sent to the WS printer. Handshaking between processes ensures that only one process is sending data to the printer at any one time.

1-20 CONFERENCE BRIDGE UNIT.

A single CBU allows the interconnection of up to five digital (via CVSD) parties. For larger conferences, the CBUs may be interconnected allowing the interconnection of up to four parties on the first and last bridge units, and up to three parties on the remaining bridge units (fig. 1-18). As many as four 3 or 4-party bridge units can be interconnected to form a 14-party conference bridge.

The low pass filter is an infinite gain multiple feedback configuration with a 5 kHz bandwidth.

The amplifier raises the signal level by 30 dB to be compatible with the following stages. The noise operated gain adjusting device (NOGAD) is a slow operating quick release circuit. When a signal consisting of speech and noise exists at its input, the output voltage is held closely to the slowly varying input noise component. The voice detector rectifies the voice signals. If only noise is present at the transmit port, the NOGAD output will be larger than the voice detector output. The comparator detects the higher noise component and causes a 15 dB loss to be inserted between the transmit and receive ports. If the voice is higher, the attenuator is removed.

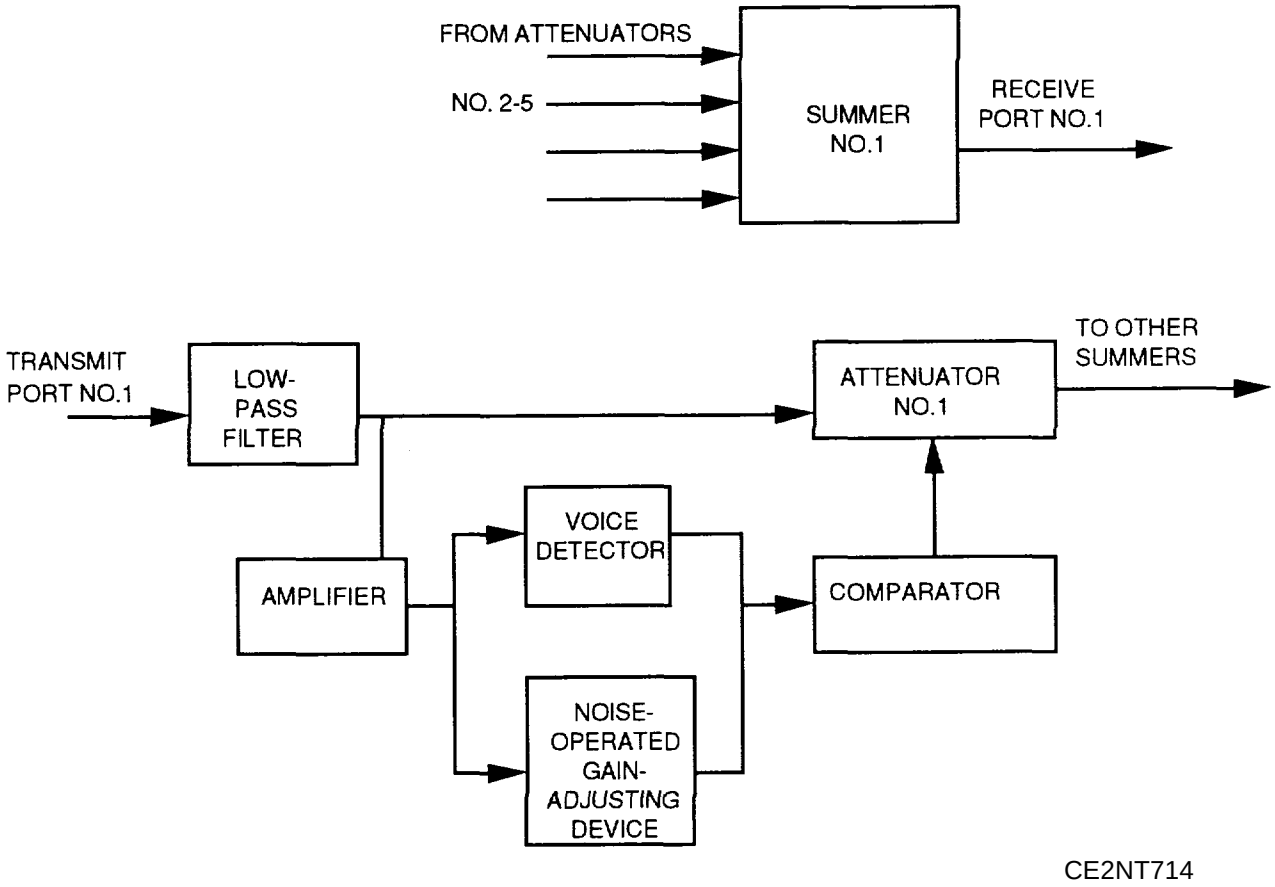


Figure 1-18. Conference Bridge Unit Block Diagram

The summer combines the signals from each of the other four transmit ports.

1-21 INTERCEPT RECORDER.

Each intercept recorder provides two recorded announcements, one for use by the processor to notify CC subscribers of an "out-of-service" condition or a "precedence violation", the other to notify subscribers of an "area restriction" or a "conference notification". The recorded announcements are connected to subscribers via the DSG and TDMX (fig. 1-19).

The recorded announcement is stored in the intercept recorder memory in a 16 kb/s, CVSD-encoded form. When the processor initiates the message read back via the SCG, the timing and control reads the data out of the memory at a 16 kb/s rate.

1-22 SWITCHING CONTROLLER GROUP.

The SCG contains the modified dual channel switching card (DCSC) and five separate device controllers (fig. 1-20). Basically, the DCSC provides the common interface between the processor and the device controllers (except COMSEC and a signaling buffer) through which all data and controls are routed. The functions of the DCSC include all level converting, command decoding, address decoding, parity checking, and handshaking routines required by the processor.

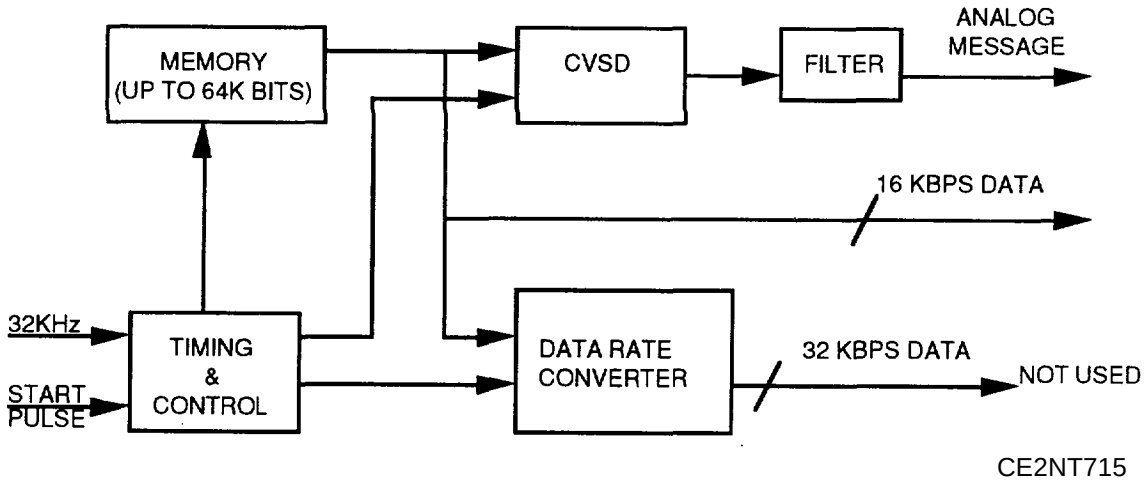


Figure 1-19. Intercept Recorder Block Diagram

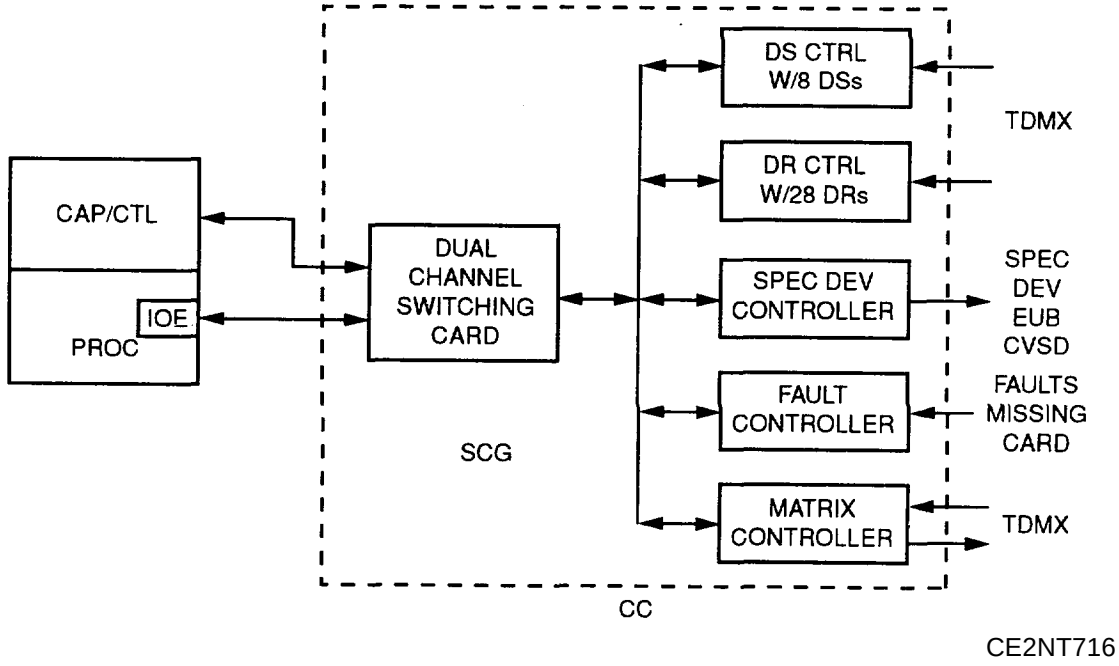


Figure 1-20. Switching Controller Group (Downsized SCG)

The individual device controllers provide the separate interfaces between the SCG and the many unique devices located in the CC equipment. In addition, certain device controllers add device identification codes, provide buffer capability, complete word formatting, and prepare the information for transmission to the processor by the DCSC. A data bus is supplied internal to the SCG which interfaces the DCSC to the common interface on the six device controllers.

1-22.1 Scanner Controller. The scanner controller provides the control functions enabling the digital scanners to transmit data to the DCSC. The scanner controller will constantly scan all the scanner devices until an active request line is found. When this happens, the scan is halted and the enable line is activated to strobe the data into the data storage portion of the scanner controller. As the data is strobed into the controller, the scanner device address will be added to it. This address is unique in any given scanner device and is determined by the device's request line.

When all the data has been received, the scanner controller activates its request line to the DCSC. At the central controller's convenience, it activates the scanner controller enable line and strobes the data out of the storage register into the processor.

1-22.2 Receiver Controller. The receiver controller provides the control functions enabling the digital receivers to transmit data to the DCSC. The receiver device scanner constantly scans all the receiver devices until an active request line is found. When this happens, the scan is halted and the enable line is activated to strobe the data into the data storage portion of the receiver controller. As the data are strobed into the controller, the receiver device address is added to it. This address is unique to any given receiver device and is determined by the device's request line.

When all the data have been received, the receiver controller activates its request line to the DCSC. At the DCSC's convenience, it activates the receiver controller enable line and strobes the data out of the storage register into the processor.

1-22.3 Matrix Controller. The matrix controller is a bidirectional device controller containing the necessary circuitry to interface the DCSC with the time division matrix.

The transmit section issues command data originating at the processor to the TDSG. Once the appropriate matrix has been selected by the matrix transmit controller, the circuitry will output the data to the selected TDSG. The receive section processes the status returned from the selected TDSG. When the matrix requesting a status output is determined, the circuitry activates the proper device enable line and inputs the status data from the matrix into the matrix receive controller. Upon receipt of the status data from the matrix, the controller activates its request line to the DCSC. At the DCSC's convenience, it activates the matrix receive controller enable line and transfers the data from the controller to the processor.

1-22.4 Special Devices Controller. The special devices controller provides the control function enabling the DCSC to transmit data to the following devices:

- EUB selector
- Master timing generator
- CVSDs
- Intercept recorder
- TGM/DTG
- Group modem
- NCMD
- TSB
- REMFM test
- Switch/Loop/Common equipment Mux/Demux
- TDMF.

At the convenience of the DCSC, four 8-bit bytes are input to the special devices controller and are temporarily stored in a 32-bit holding register. The first two data bytes contain the desired device type and device address. The sender controller decodes the device address of a discrete device enable line and activates this line, outputting the data in a serial stream to the proper device.

1-22.5 Fault Controller. The fault controller contains the scanning and digital processing logic which detects and formats any change in device status and the control logic which enables the status change to be reported to the processor through the DCSC.

1-22.6 Signaling Buffer Controller. The SBC provides the interface between the trunk signaling buffers (TSB)/digital in-band trunk signaling buffer (DSB) and the processor. The SBC directs data to the proper signaling buffer as received from the processor. In addition, data from each buffer is formatted for transfer to the processor (fig. 1-21).

The transmit/receive coordinator provides the overall coordination of data flow over the bidirectional bus connecting the SBC to the processor.

The transmit buffer stores up to four data bytes (32 bits) from the processor. Parity on each byte is tested, but not saved. The command parity error detector tests parity on all command addresses and reports to the processor via an interrupt.

The transmit control logic (TCL) controls the transfer of the message from the processor to the TSB. The TCL recognizes that the command is intended for the SBC, interprets the command, and delivers the command to the proper signaling buffer.

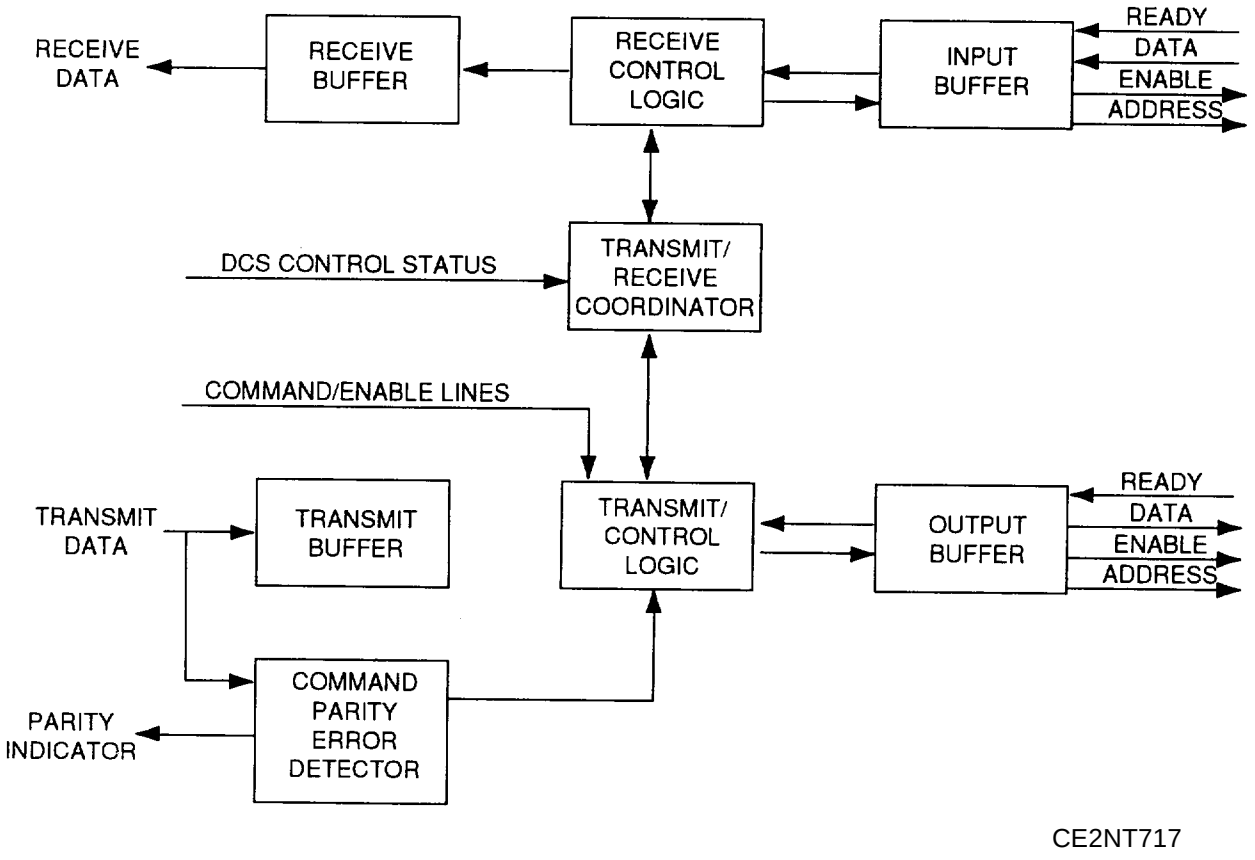


Figure 1-21. Signaling Buffer Controller Block Diagram

The output buffer determines when a signaling buffer can accept data from the processor. Upon ready, the output buffer delivers the data to the signaling buffers.

The receive control logic (RCL) determines when a signaling buffer has data to transfer to the processor. The signaling buffer address is added to the data transferred to the processor to identify the responding unit. The output of data to the processor is controlled by the RCL.

The receive buffer stores up to four data bytes (32 bits) for transfer to the processor. The input buffer accepts data from the signaling buffers under control of the RCL.

1-23 COMSEC CONTROLLER.

The COMSEC controller is a bidirectional device controller containing the circuitry necessary to perform a serial/parallel data conversion and to operate the interface control unit (ICU).

The first byte of every message contains an indication of the number of characters in the message. A character counter is set according to this information to determine the last character. When the last character is detected, the transmit buffer status is reset and the transmission to the ICU is initiated. The COMSEC controller accepts and buffers up to six characters per transmission. When the ICU is ready, the data characters are parallel-to-serial converted, a parity bit is attached to each character, and the message is transmitted in contiguous nine-bit bytes.

Data from the ICU is serial-to-parallel converted and stored in eight-bit bytes in the receive data buffer. The parity bit is removed and checked before data is entered into the receive data buffer.

1-24 LOCAL TIMING GENERATOR.

The LTG consists of two identical units. One unit is designated as the master "A" unit, and the other unit is the redundant "B" unit. Each unit of the LTG interfaces with the MTG and consists of seven functional areas (fig. 1-22). Four LTGs are used on the CC (two designated RED and two designated BLACK). .

The differential input line receiver provides the 90 ohm termination for each of the three clock frequencies plus the 100 Hz synchronizing pulse received from the MTG.

Binary counters are used to generate square waves for the required clock outputs.

The Johnson counter is used to generate those clock frequencies requiring duty cycles of 25 percent and other special pulses, such as the 32 kHz frame sync pulse.

Drivers are provided for each clock output. The driver outputs from each unit in the LTG are ORed together. The RED LTG outputs are buffered through LTBF circuit cards located in close proximity to the LTGs to reduce the length of each clock line as well as the load.

Fault logic and switch over circuits are provided for each unit of the LTG. When a failure occurs on the "A" unit, the output drivers are turned off and a fault indication is sent to the SCG for transfer to the processor. In addition, fault signals are sent to the "B" unit of the LTG, enabling the driver outputs for that unit.

When the "A" unit of the LTG is replaced, a power-on reset circuit in the "A" unit prevents a B-to-A unit switchback from occurring until fault logic on the "A" unit has been operating long enough to determine that the "A" unit is good. Upon completion of the power-on reset, and with the "A" unit good, the switchback from the "B" redundant unit to the "A" master unit occurs. If the "A" unit replacement was bad. no switchback occurs after the power-on reset.

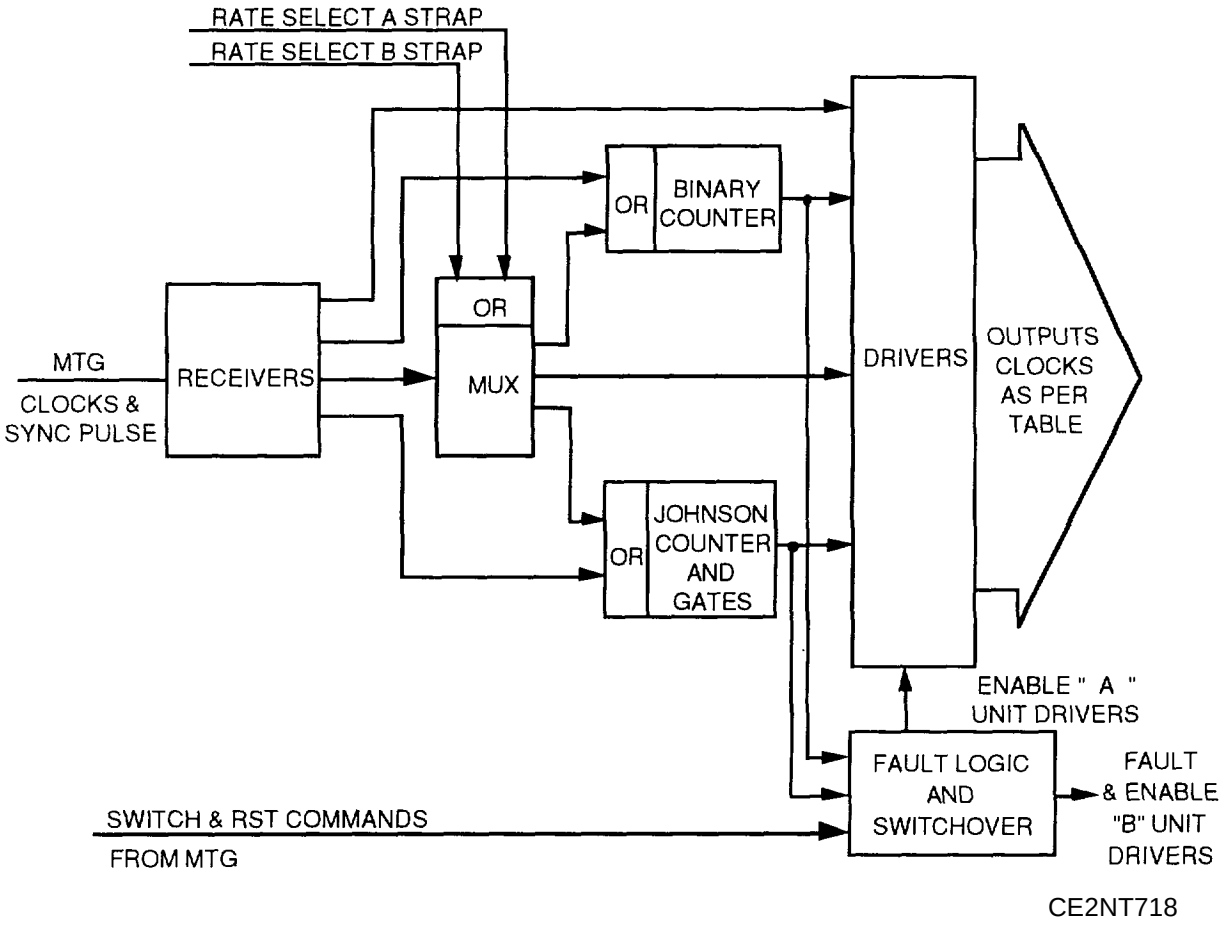


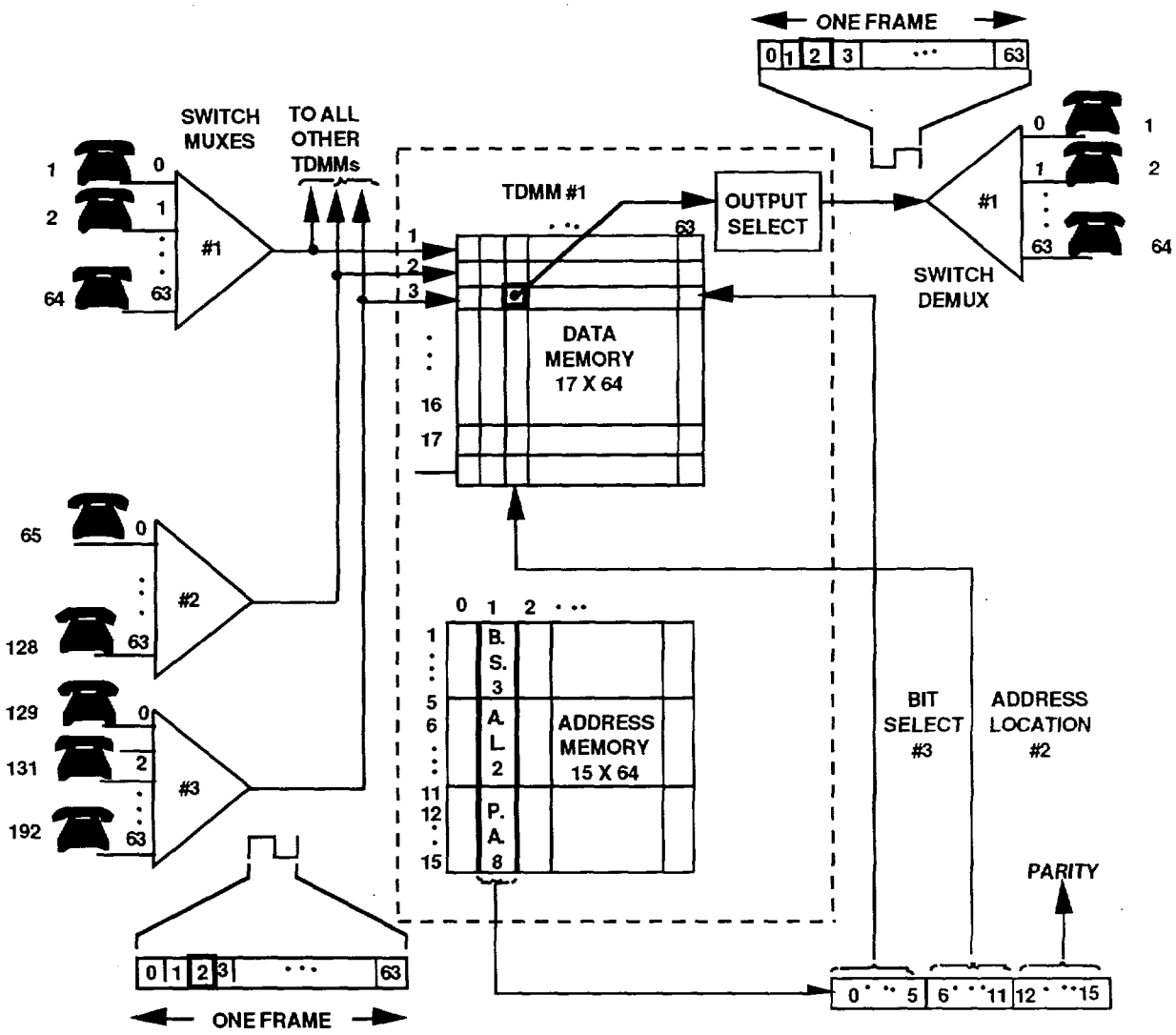
Figure 1-22. Local Timing Generator Block Diagram

1-25 TDMX MANAGEMENT AND CONTROL.

1-25.1 Time Division Matrix. The TDMX management control is provided by the central processor's circuit switch on-line control and operational program (CSOLOP) through the matrix controller.

The TDMX consists of a group of 15 TDMMs. The TDMM performs the time division switching of multiplexed data streams originating at the switch multiplexers or DSG. Each TDMM contains a 64 x 17-bit storage area for subscriber data bits and a 64 x 15-bit storage area for address location bits. In addition, each TDMM contains all the logic necessary to interface with the SCG and interpret the connection and control commands from the processor to perform the time division switching and memory check functions.

The TDMX operation can best be explained using a typical half-connection which is shown in figure 1-23. In this example, a half-connection will be made from bit select number 3, address location number 2 (subscriber number 131) to bit select number 1, address location number 1 (subscriber number 2). Each group of 64 subscribers is multiplexed by the switch muxes into a single 64-channel, 1.024 Mb/s digital data stream. The data stream from each switch mux is bussed to every TDMM where the 64 data bit positions (one for each subscriber) are stored in the data memory at the appropriate bit select location. In addition to the maximum of 15 data streams from the switch muxes, two 64-channel data streams originate at the two DSGs. The DSG output data streams are also bussed to every TDMM in the switch. Thus, the CC shelter contains 15 TDMMs, each of which contains a 17 x 64-bit data memory. All data memories are identical and contain an input data bit from every subscriber.



HALF CONNECTION FROM BIT SELECT #3, ADDRESS LOCATION #2 (ORIGINATOR) TO BIT SELECT #1, ADDRESS LOCATION #1 (RECIPIENT)

CE2NT719

Figure 1-23. Typical Half Connection

The half-connection command from the processor designates the originator and the recipient of the call. The TDMM, recognizing itself as the recipient, stores the originator address in the address memory at the recipient location. In the example, the originator address (bit select 3, address location 2) is stored in the address memory of TDMM number 1 (bit select 1) at location 1 (address location 1). If this were a full-connect command, bit select 1, address location 1 would be stored in the address memory of TDMM 3 at location 2. The address memory is a 15 x 64 memory.

The 64 locations in the address memory are read out synchronously to the data bits out of the output selector. For instance, the address in location 1 of the address memory is read out and then validated with the parity bits. The bit select address stored determines the row in the data memory to be accessed, and the location address stored determines the column in the data memory. The data bit at the intersection of these two addresses is output in time slot 1 (location 1) to the switch demux. This process is repeated for all 64 locations. The switch demux decombines the 64-channel bit stream into 64 individual data channels. The data bit at location 1 is then output to subscriber 2. Thus, subscriber 2 listens to subscriber 131

The timing and control circuitry shown in the block diagram of figure 1-24, decodes the 40-bit serial command from the SCG. The SCG command buffer converts the command word to a parallel format. The memory ID and A/B bit select comparator and A/B channel counter comparator decode the bit select and address location fields, respectively. The bit select is decoded by comparing against a preset program register, and the address location is decoded by comparing against the output of the channel counter which cycles through the 64 possible states. The timing and control logic decodes the command, signals connect/disconnect completion, and selects the address for storage in the address memory. The counter check verifies that the location address is stored in the proper address memory location and the parity check insures that the command has been properly transmitted across the processor-TDMX interface. The parity check is performed prior to the address storage in the address memory.

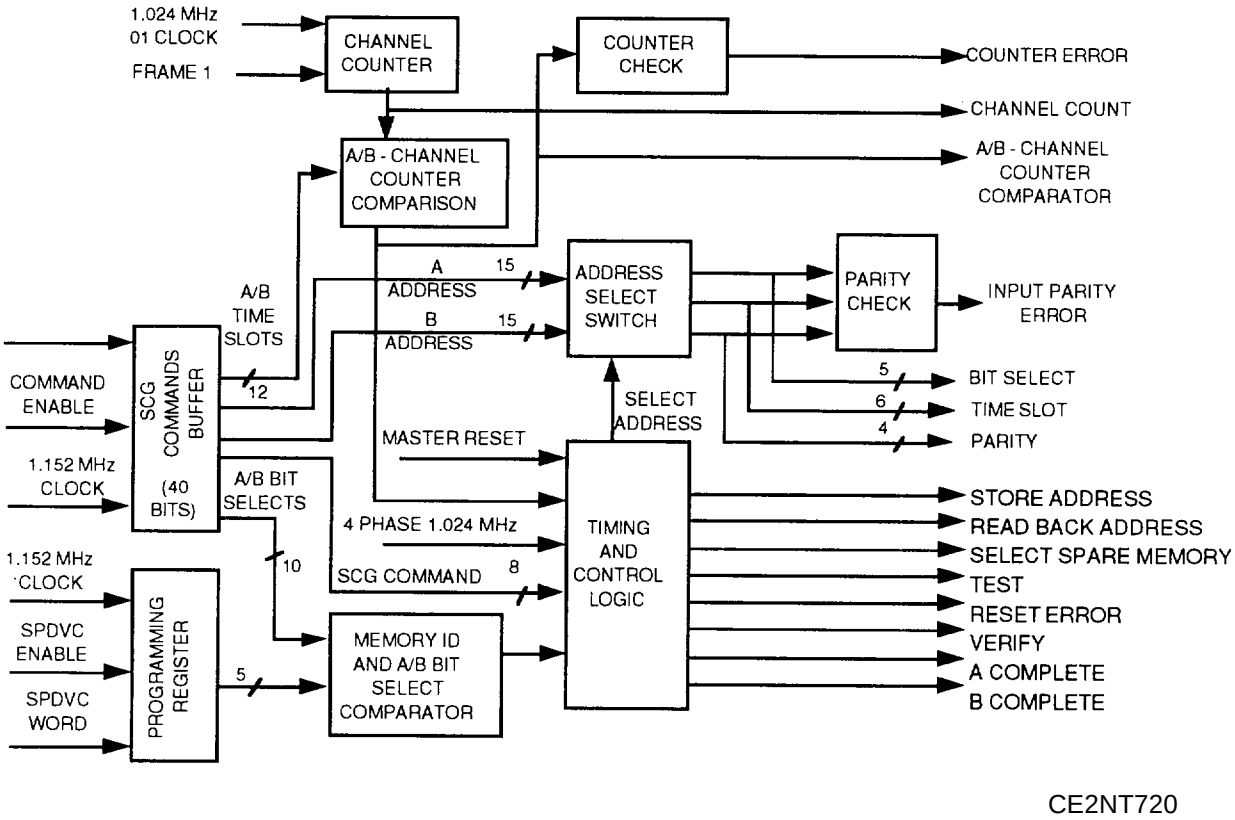


Figure 1-24. Timing and Control Circuitry Block Diagram

Switching and fault detection circuits are presented in the block diagram of figure 1-25. The 15-bit connection commands are stored in the 64 x 15 address memory and the subscriber data bits are stored in the 64 x 17 data memory. The addressing of these memories is controlled by the address select switch and memory address register. The parity check monitors the output of the address memory to insure proper storage and readout. A stored address parity error is reported upon detection of a parity error. Bit select switch #1 selects the data bit for output to the switch demux. The data bit selected by bit select switch #2 is compared against the output data bit in the comparator. An output data select error is returned to the processor if the two data bits do not match. The data summing adds the 17 bits in the addressed location address. This sum is compared with the same data summation from each of two adjacent TDMMs. A data memory error is returned to the processor if both comparisons are invalid. The "read back location buffer" returns the address stored in a location of the address memory when commanded by the processor.

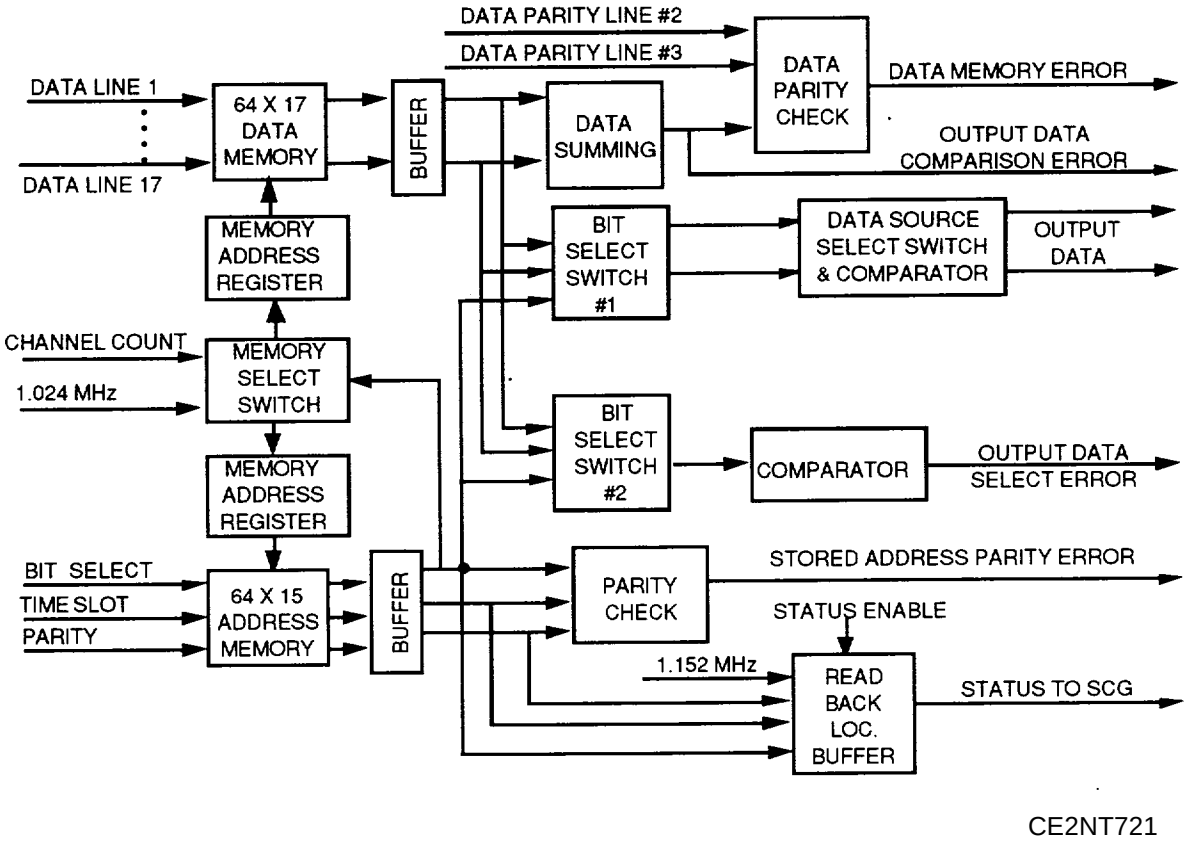


Figure 1-25. Switching and Fault Detection Block Diagram

1-26 LINE DRIVER INTERFACE (LDI).

The LDI cards perform logic level conversion between TTL level signals and low-level, balanced bipolar signals. Both TTL to bipolar and bipolar to TTL are provided as required in the application.

1-27 CENTRAL PROCESSOR GROUP (CPG).

Refer to TM 11-5895-1327-34-1 for detailed descriptions of the CPG.

1-27.1 General. The CPG is a high speed, general purpose, modular-type computer. It provides multiple program level control, memory expandability, multiple general-purpose registers, and independently controlled I/O communications.

The CPG consists of a status and control panel, status and control panel interface cable, central processor unit (CPU), solid state memory (SSM) units, input/output unit (IOU) and CPU circuit card assemblies (fig. 1-26).

1-27.2 Status and Control Panel. The status and control panel contains operator controls and indicators required by an operator to initialize and monitor system operation. The controls and indicators are arranged for rapid identification of individual functions. Controls are provided to initiate:

- Restart
- Program load
- Program test.

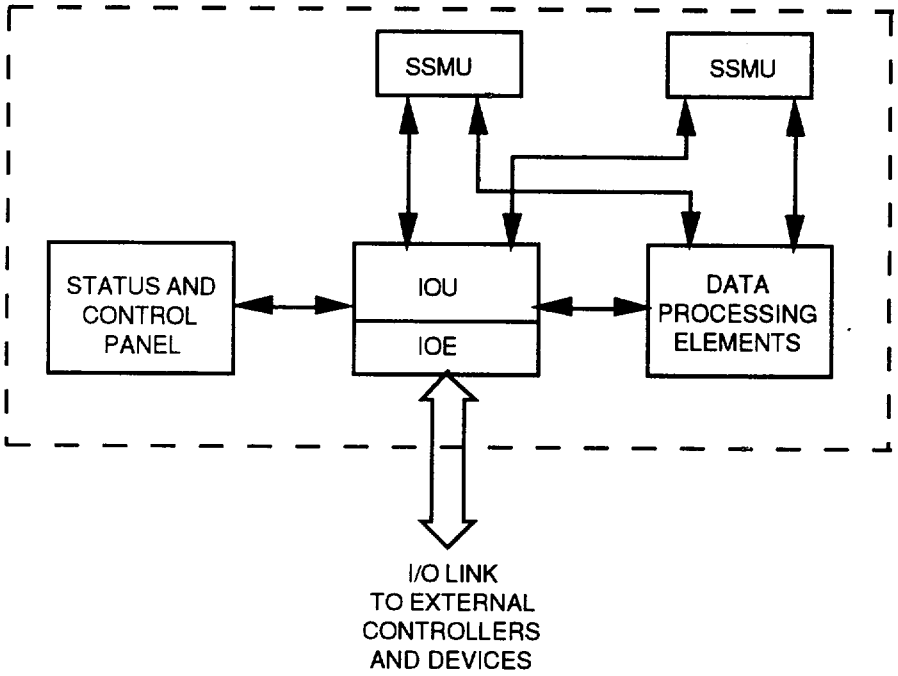


Figure 1-26. CPG Functional Block Diagram

Indicators for DIAGNOSE STATUS, I/O ERROR and MEMORY PARITY are also provided. An explanation of the status and control panel controls and indicators is given in Chapter 3.

1-27.3 Central Processor Unit. The CPU consists of an enclosed card cage assembly with seven circuit card types (12 circuit cards total). All signal connections transmitted from and received by the CPU pass through the card cage assembly I/O connector plate to the nest backplane. The CPU is powered by regulated +5 Vdc applied directly to the CPU card cage backplane. The CPU provides all the computer associated data processing operations such as, arithmetic, logic, control, timing, memory, and I/O functions of the CPG. The hardware requirements for these functions are the various circuit cards in the CPU. Refer to TM 11-5895-1327-34-1, Chapter 2, for detailed descriptions of these circuit cards. The CPU circuit card types consist of:

- Arithmetic Logic Units
- Microsequencer
- Solid State Memory
- Front Panel Interface
- Micromemory
- I/O Exchange
- Dual I/O Expander.

There are several functional elements in the organization of the CPU with intercommunications between the elements via a data bus. The data processing elements are: instruction controller, program level controller, arithmetic section, memory interface controller, and process registers, SSM, and an input/output (I/O) unit (fig. 1-27).

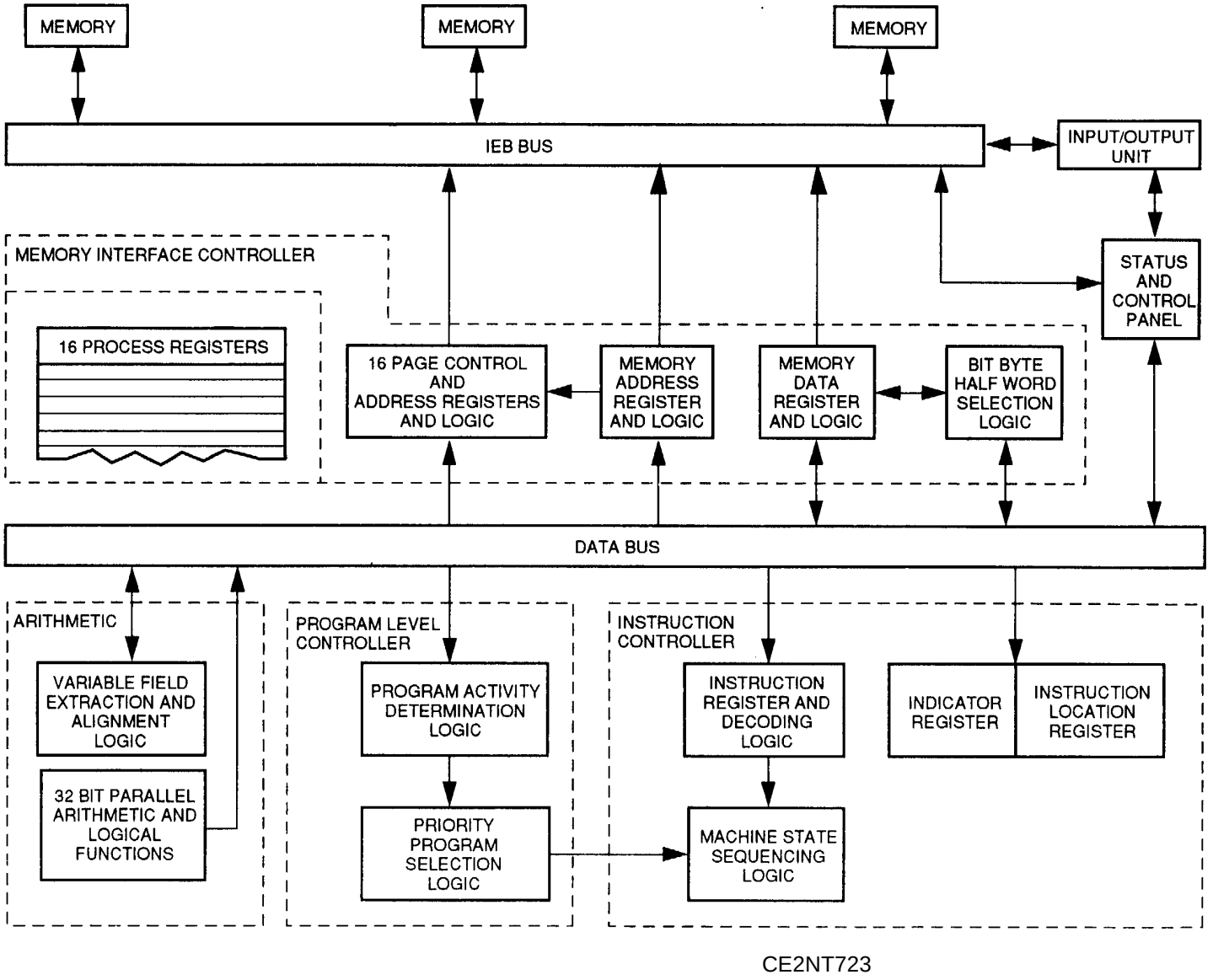


Figure 1-27. CPU Functional Block Diagram

1-27.3.1 Instruction Controller. The instruction controller controls the sequence of operations within the CPU. The instruction controller contains an indicator register with flag assignments that indicate the program status of the data processing system. The instruction controller also contains an instruction location register, which keeps track of the current instruction address, and an instruction register and decoding logic section, which stores and decodes the instruction being executed.

1-27.3.2 Program Level Controller. This controller contains the logic that controls the operation of one of the key real-time functions of the processor. This logic updates priority queue registers and checks them to ensure that the highest available priority program in the queue is running. The controller also contains control logic for switching program levels.

1-27.3.3 Arithmetic Section. The arithmetic section contains a high-speed, 32-bit parallel adder, as well as field extraction and alignment logic that makes the variable field operations of the processor possible. The variable field operations are used to pack the memory data fields and to provide the flexibility of data processing on a bit, byte, or half-word basis.

1-27.3.4 Memory Interface Controller. The memory interface controller contains memory address register and logic, memory data register and logic, page control and address registers and bit, byte, and half-word selection logic.

The memory address and memory data registers are normally associated with a memory-processor interface. The page control and address registers contain the 16-page address associated with the active program level. Each page address accesses up to 2048, 32-bit (plus parity) words. The pages may be ordered in any sequence, providing flexibility in the organization and relocation of the program and data.

The bit, byte, and half-word selection logic is used to select regularized short fields for processing by the arithmetic section or for transfer to another block. The capability to select directly 1, 8, or 16 bits from a 32-bit word, complements the variable field capability of the arithmetic block and permits flexibility in the storage and processing of data files. Byte select for memory interface occurs only during the write or read mode.

1-27.3.5 Process Registers. Sixteen 32-bit process registers are available to the active level program. The registers are actually random-access memory elements which operate with a cycle time of 200 nanoseconds. These high speed memory elements may be used as accumulators, as index registers, or to hold instructions during the execution of program loops.

1-27.3.6 Solid State Memory. The SSM provides the random-access, high-speed memory facility for the CPU. The SSM accepts and responds to control signals, accepts and stores data, generates responses, and transmits data to the various elements of the CPU.

Each SSM module has a storage capacity of 1,048,576, 36-bit words organized into two 524,288 x 18 bit sections (physically contained on one printed circuit card). The SSM uses a word format consisting of 32 data bits and four parity bits. Each CPU has the capacity to configure up to four SSM modules (fig. 1-28). In addition to a master reset, the SSM operates in the following mode:

- Write lower byte
- Write upper byte
- Write word
- Write double word
- Read word
- Read double word.

In the read mode, the SSM reads and transmits data stored in the specified address. In the write mode, data is stored in the specified address by the SSM. The SSM uses a 24-bit address for addressing up to 4,194,304 words of memory.

The SSM has a capability for external memory backup and control to provide for momentary power loss or shutdown. Since there are no security requirements for the preservation of RAM data, this capability is not implemented.

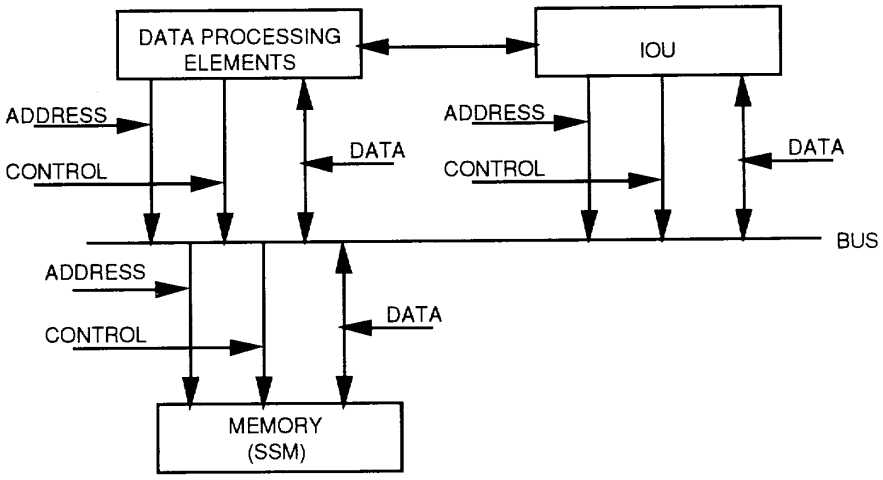


Figure 1-28. Solid State Memory Interface and Access Characteristics

1-27.3.7 Input/Output Unit. The IOU is used by the CPU to provide control of communication between the SSM and the peripheral equipment. The IOU consists of the input/output controller (IOC). data exchange units, three real-time clocks, and the status and control panel logic (fig. 1-29).

All of the IOU device channels have identical capabilities. The possible I/O modes are alarm, input word (four 8-bit bytes), output word (four 8-bit bytes), input byte (eight bits), and inactive.

Each device has a keyword and a terminate word that defines the modes as well as starting memory location of data and quantity of data to be transferred. Devices may interrupt the CPU when an I/O sequence has been completed. Interrupts may be stacked and the interrupt of any I/O device can be directed to any program level.

All I/O operations are under control of software through the use of keywords, terminate words, and I/O commands. These are privileged instructions that allow direct commands to be sent to a device, or allow status to be obtained from a device. The commands are DEV (device command), DEX (device command and exit), ITR (input to register command), and OFR (output from register command).

Status information is also available whenever a device interrupts the computer. All I/O operations on every channel are checked for correct input parity. Every byte of I/O has odd parity. Memory parity is also checked whenever data is accessed prior to being sent over the I/O lines, as well as parity being generated when data is placed in memory. A parity error or any other error detection results in an I/O error interrupt.

Each peripheral device serviced has a fixed device address, and servicing is based on a priority scheme.

1-27.3.8 Input/Output Controller. The IOC is responsible for the multiplexing of data between the memory and various other devices. The IOC receives its command from the keyword interpretation logic and from the processor via the I/O command interpretation logic. Either of these logic sources controls the interface controls generation logic. Data that is transferred via the input/output dc bus are assembled or disassembled into words or bytes in the byte/word assembly-disassembly logic. The direct interface request for service from peripheral devices, or commands to devices, are transmitted by the device request/select logic.

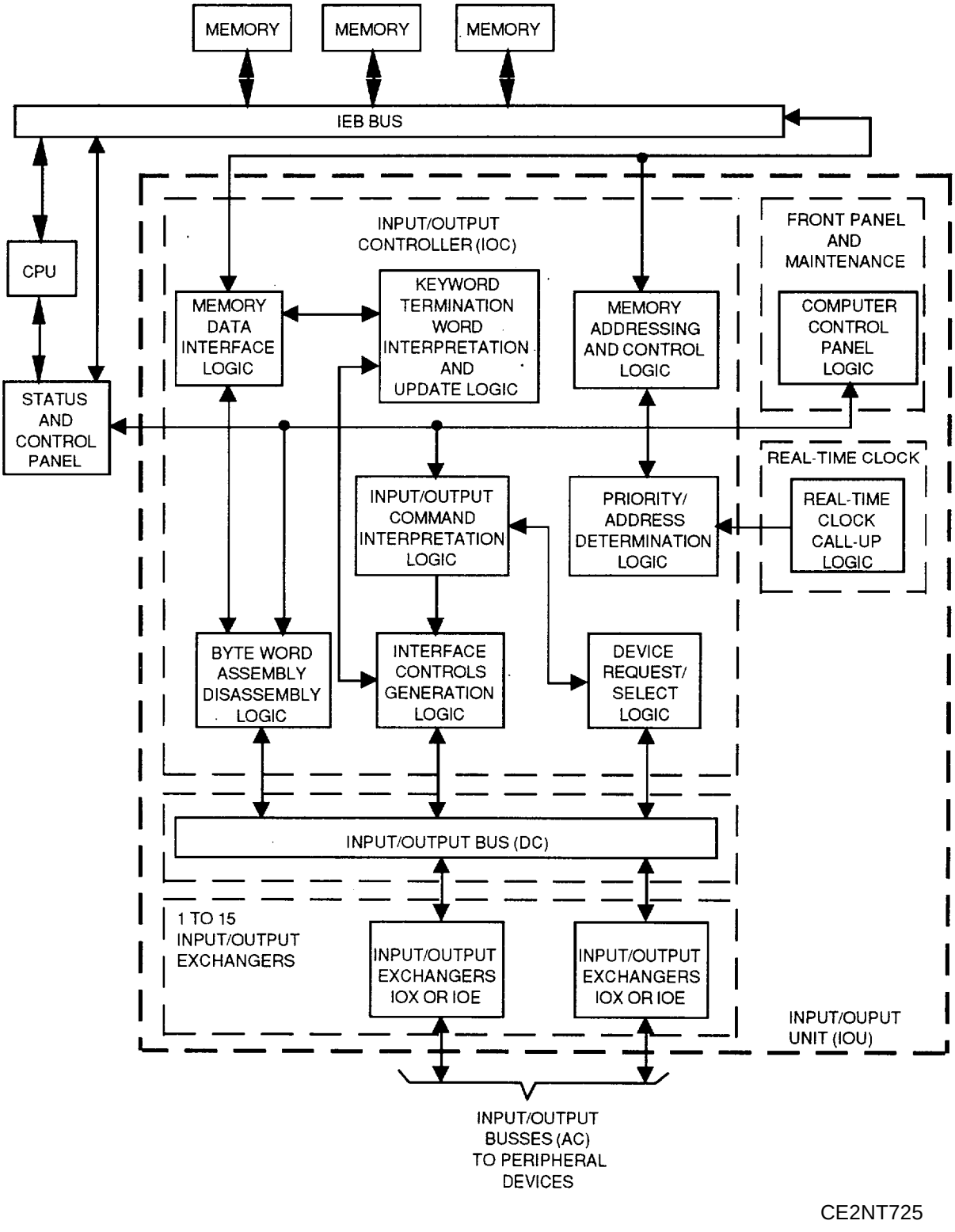


Figure 1-29. input/output Unit Functional Block Diagram

The priority/address determination logic and the memory addressing and control logic control priority and memory-addressing functions. The memory data interface logic administers the actual reading and recording of data into the memory.

1-27.3.9 Data I/O Exchange Units. Data may be exchanged with peripheral devices either directly via the input/ output dc bus using an input/output exchange (IOE), or via the longer input/output ac bus using an input/output extender (IOX). The IOE is used when devices are less than 50 feet from the IOE. The IOX is used when devices are greater than 50 feet, but less than 330 feet from the IOX.

1-27.3.10 Real-Time Clocks. The IOU uses three real-time clocks within its input/output processor (IOP) section. The IOP refers to a processor within the CPU dedicated to 10 functions. The primary function of the real-time clocks is to define either the time-of-day or intervals of fixed or variable duration. They also monitor the responsiveness of the IOP and program execution. The real-time clocks appear to software as three separate peripheral devices and are completely under program control. The IOC sees them as high priority devices that require count monitoring, but no memory data transfer. All three real-time clocks have a count resolution of 1 millisecond.

1-28 POWER GROUP, CC CIRCUIT SWITCH.

1-28.1 General. The power group provides the total power requirement for the CC circuit switch (figs. 1-30 and 1-31).

Prime power voltage for the CC shelter is ac and is provided by a 10 kW diesel-powered generator. Normally, the shelter operates from the generator prime power. A portion of the prime power ac voltage is converted to 26.5 Vdc at the power bay in each shelter. This voltage is used to charge two 12 Vdc batteries and develop a 24-Vdc bus for powering all the switch operating equipment. When the prime power becomes unavailable or it cannot be accessed, the batteries take control of the 24-Vdc bus. The batteries provide dc power, for up to 10 minutes, for maintaining the operation of the switch. If normal shelter operation is interrupted by a loss of ac power and ac power cannot be accessed by the shelter, the battery power can be replaced by connecting the dc bus to the shelter vehicle's (HMMWV) 200-ampere alternator to extend the operating time of the switch. However, because the vehicle provides only dc power to the shelters when ac power is not available, none of the ac-powered equipment in the shelter, such as the ECU or heater, the intercom, the main lights, and ancillary equipment connected to the utility outlets, is operational.

1-28.2 CC Shelter Power Group.

1-28.2.1 AC Power. AC power (120 Volts, single phase, 60 Hz) enters the shelter through the PEP. At the PEP, a portion of the power passes through circuit breaker CB2, which provides protection for the shelter ECU. The remaining power passes through an ESA filter and an EMI filter. The ESA filter suppresses input line transients. The EMI filter eliminates the effects of the emissions generated within and external to the shelter.

Filtered ac power from the PEP goes to the main power and control (ac) circuit breakers CB3 and CB4 respectively, on the ac power control panel. The control circuit breaker provides protection to the ac voltage and frequency meters installed on the power control panel, while the main power circuit breaker provides protection to all other ac-operating equipment except for the ECU. At the ac power control panel, a part of the ac power goes out of CB3 to the main lights through circuit breaker CB7, while the remaining part goes out to the ac circuit breaker panel limiting the maximum output voltage of the filter to values that cannot damage the shelter equipment. At the ac circuit breaker panel, a part of the ac power goes through circuit breaker CB6 to the regulator/battery charger, while the remaining part goes to the following ac circuit breakers: CB5 - UTILITY/ INTERCOM, CB24 - PS1, CB31 - PS2, and CB35 - OPU/PTR.

1-28.2.2 Normal DC Power. The regulator/battery charger converts the 120-Vac power to regulated 26.5-Vdc power. The output of the regulator/battery charger takes the form of a dc bus after it passes through battery charger output circuit breaker CB11. One of the uses of the bus is to maintain a floating charge on the battery

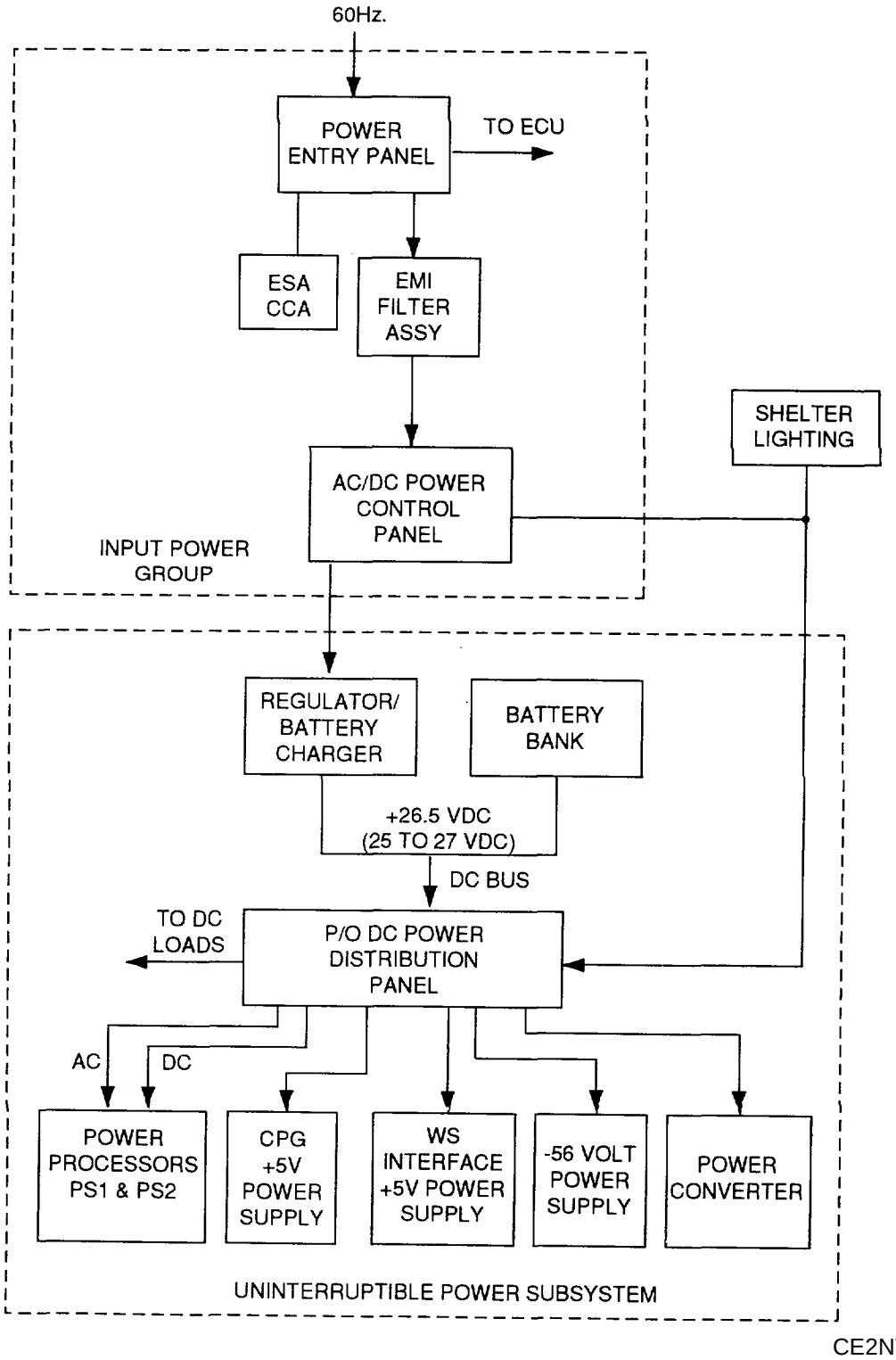


Figure 1-30. Power Group Block Diagram

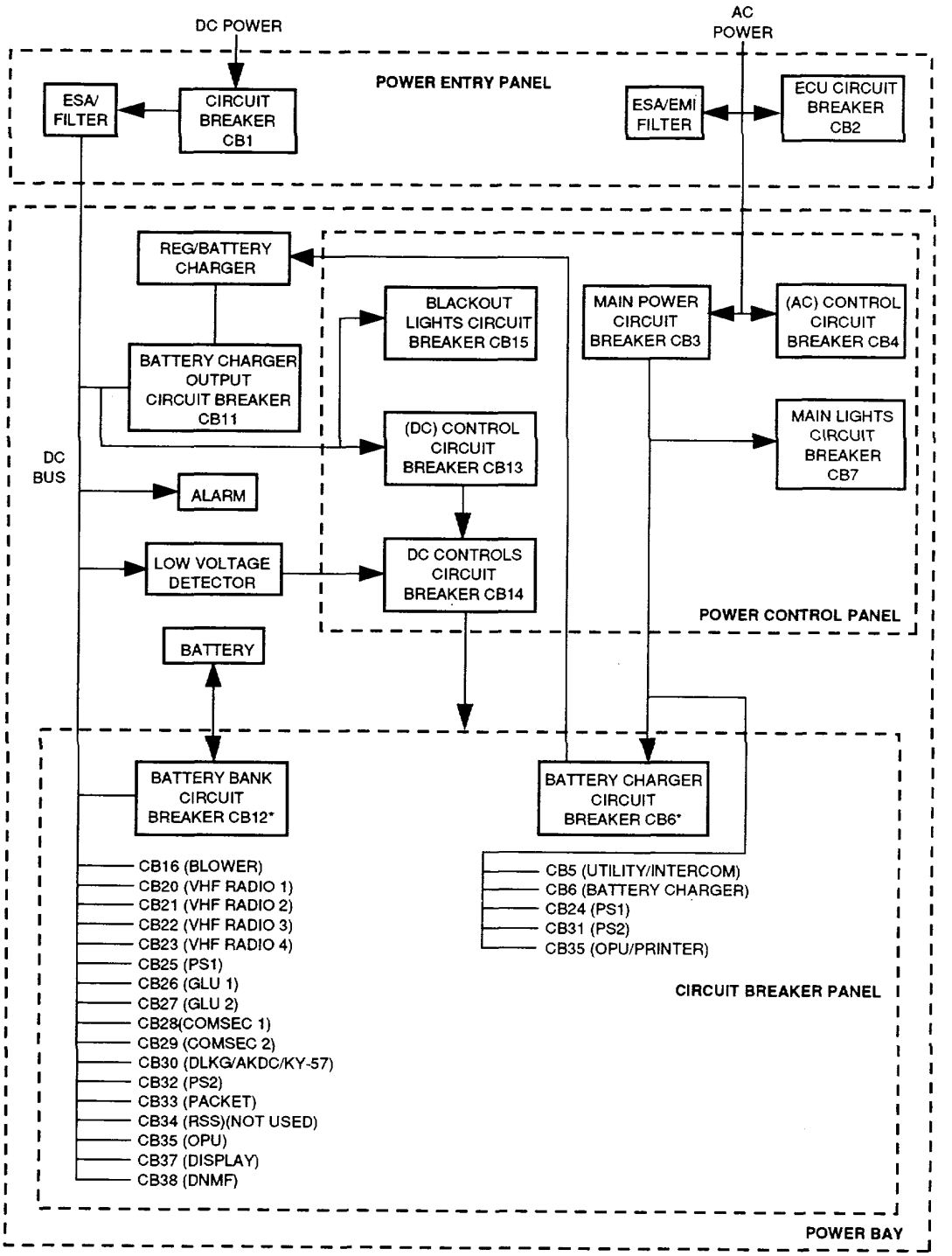


Figure 1-31. CC Shelter Power Flow Block Diagram

used for a temporary dc backup. A part of the dc bus at the output of CB11 goes to the dc power control panel, while the other part goes to the audible alarm, a low voltage detector, and the dc circuit breaker panel. The audible alarm sounds if the dc power from the regulator/battery charger is interrupted. At the dc power control panel, the dc bus goes to control (dc) circuit breaker CB13, and blackout lights circuit breaker CB15. At the dc circuit breaker panel, the dc bus goes to the following dc circuit breakers: CB16 - BLOWER, CBs 20 through 23 -VHF RADIOS 1 through 4, CB25 - PS1, CB26 - GLU1, CB27 - GLU2, CB28 - COMSEC1, CB29 - COMSEC2, CB30 - DLKG/AKDC/KY57, CB32 - PS2, CB33 - PACKET, CB34 - RSS, CB36 - OPU, CB37 - DISPLAY, and CB38 - DNMF.

The dc line at control circuit breaker CB13 in the dc power control panel goes to dc controls circuit breaker CB14. This circuit breaker, together with all circuit breakers at the circuit breaker panel, have the capability of switching off when the dc power in its line drops to 20 Vdc. All breakers are tripped in common by a low voltage detector. CB14 operates with the low voltage detector and trips circuit breakers CB21 through CB28 to switch them all off.

1-28.2.3 Backup DC Power. Emergency backup dc power (uninterruptible) is provided by two lead-acid batteries connected to the dc bus. It automatically provides up to 10 minutes of power to the dc bus if the output from the regulator/battery charger fails. If the regulator charger output fails, the operator must immediately connect backup dc power from the vehicle to the dc bus. When dc power from the vehicle is connected and turned on, it goes through circuit breaker CB1 and an ESA filter before going on to the dc bus. The vehicle dc power obtains control of the dc bus and starts recharging the battery to its full capacity. Once the battery reaches its full charge, the vehicle dc power maintains a floating charge on the batteries. If the dc bus failure was caused by an ac power failure, the ECU, intercom, workstation printer, and equipment connected to the utility outlets which require ac power for operation become nonfunctional.

1-28.3 AC/DC Power Control Panel. The ac/dc power control panel is the control and power monitor center within the shelter(s) (figs. 1-32 and 1-33). The components on this panel provide the means for controlling and monitoring ac and dc power. The panel is located within the shelter to provide convenient operator access to the controls as well as visibility of meters and indicator lights. The ac/dc power control panel is comprised of the following components:

1-28.3.1 Power Alarm Group.

1-28.3.1.1 Phase Rotation Detector. During the application of prime ac power to the distribution network, the phase rotation of the input power is monitored to ensure that the correct phase rotation relationship exists. Phase detection circuitry is provided for this purpose. Detection of an incorrect phase relationship or loss of one or more phases causes the following:

- The main ac circuit breaker is not allowed to maintain the on condition
- An audible and visual phase sequence alarm is activated.

1-28.3.1.2 TEST Pushbutton Switch. Turns on audible alarm when pressed. Alarm shuts off when released.

1-28.3.1.3 Audible Alarm Indicator. Sounds when fault is detected in power system or when POWER ALARM TEST push-button is pressed.

1-28.3.1.4 AUDIBLE ALARM OFF Pushbutton Indicator. Indicator goes on when pressed to disable alarm for most fault conditions. Must be pressed second time to enable alarm. Does not disable battery exhaust fault alarm.

1-28.3.2 DC Group.

1-28.3.2.1 BUS VOLTAGE Meter. Shows voltage of dc bus. During normal operation reading should be 25 to 28 Vdc.

1-28.3.2.2 CONTROL Circuit Breaker. Protects dc control circuit. Trips off and displays white band when control is overloaded.

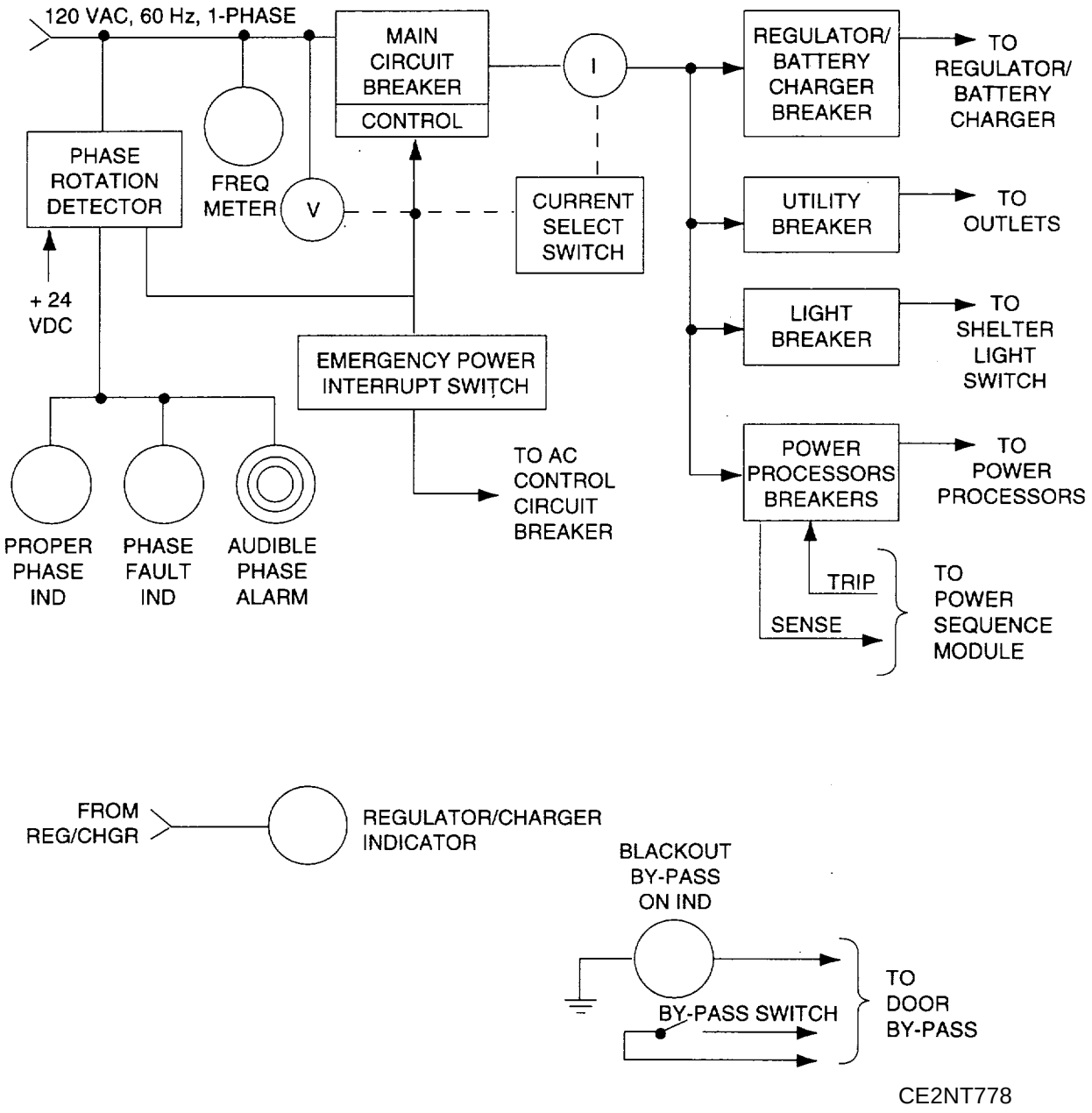


Figure 1-32. AC/DC Power Control Panel Interface Diagram (AC Section)

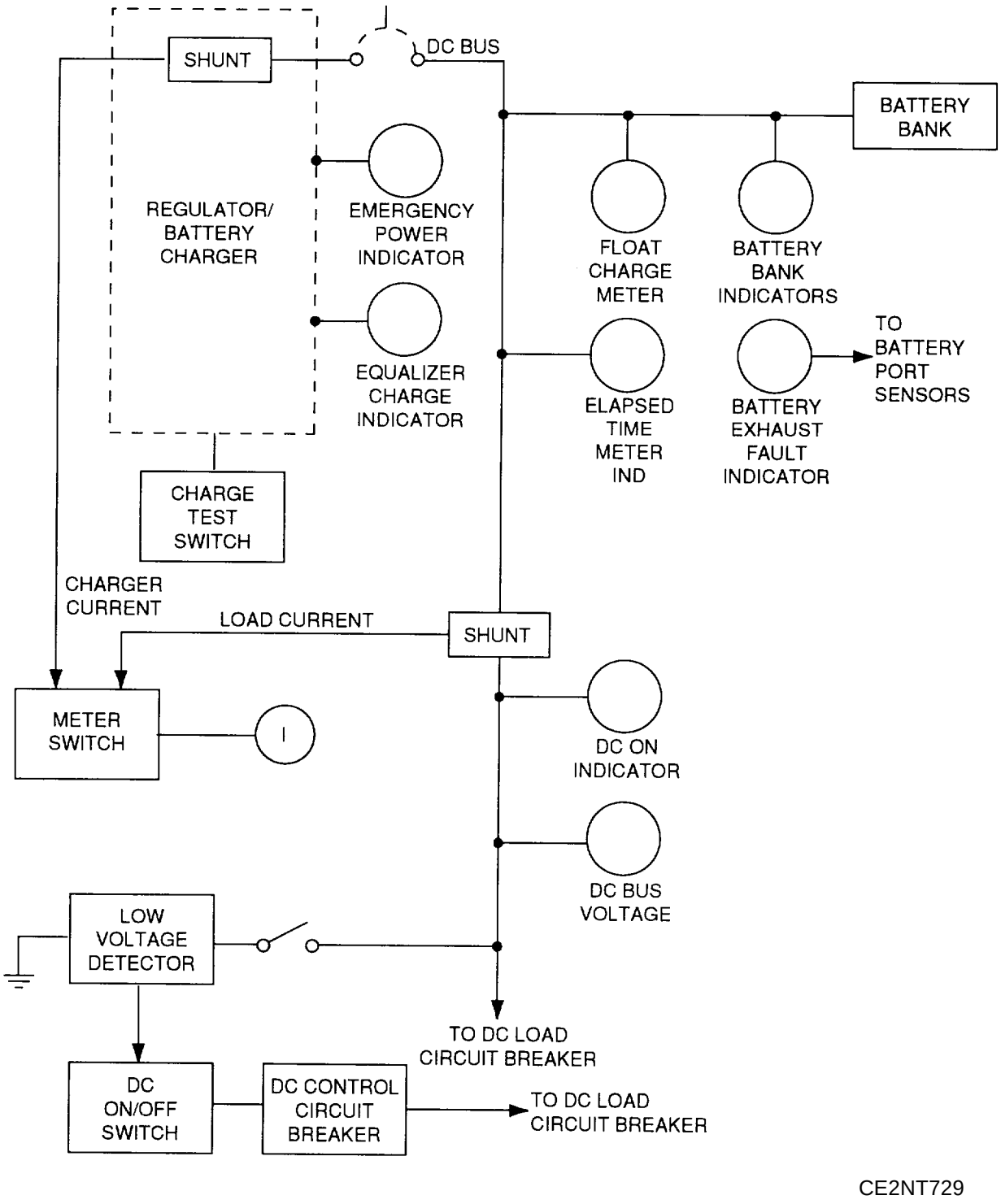


Figure 1-33. AC/DC Power Control Panel Interface Diagram (DC Section)

1-28.3.2.3 ELAPSED TIME Counter. Shows total amount of time (in hours) that dc power has been on.

1-28.3.2.4 EQUALIZING CHARGE. Indicator is on when pressed. Starts charge equalizing cycle pushbutton indicator.

1-28.3.2.5 CURRENT SELECT LOAD/CHGR Toggle Switch. Selects which current is to be read by CURRENT meter: CHGR position for regulator/battery charger current, LOAD position for dc load current.

1-28.3.2.6 CHARGE TEST Pushbutton. Used to check charge of batteries to determine if equalizing switch charge cycle must be started.

1-28.3.2.7 DC ON-OFF Pushbutton. Turns on dc power subsystem when pressed. Indicator is on when dc power is on. Must be on before any dc circuit breakers can be set to on.

1-28.3.2.8 EMERGENCY POWER Pushbutton Indicator. Indicator is on when main ac input power has failed or when operating on emergency backup power and no power output is detected from the regulator/battery charger. Indicator is on when pressed to check lamp.

1-28.3.2.9 DC CONTROLS Circuit Breaker. Applies power to and provides protection for dc power breaker subsystem.

1-28.3.2.10 BATTERY ON BUS Pushbutton Indicator. Indicator is on when battery is on dc bus. Indicator is on when indicator is pressed to check lamp.

1-28.3.2.11 EMERGENCY LIGHTS TEST/NORMAL Toggle Switch. Applies power to and provides test for shelter emergency lights.

1-28.3.2.12 BATTERY EXHAUST FAULT Pushbutton Indicator. Indicator is on when battery vent cover is closed. Indicator is on when pressed to check lamp.

1-28.3.2.13 BLACKOUT LIGHTS Circuit Breaker. Applies power to and provides protection for blackout lights. 1-28.3.2.14 BLACKOUT BYPASS Pushbutton Switch. Indicator is on when pressed and bypasses blackout indicator lighting system allowing main shelter lights to stay on when door is opened.

1-28.3.2.15 CURRENT Meter. Depending upon position of CURRENT SELECT switch, shows (in amperes) either dc load current or current from regulator/battery charger.

1-28.3.3 AC Group.

1-28.3.3.1 REGULATOR CHARGER ON Pushbutton Indicator. Indicator is on when regulator/battery charger power is on. Indicator is on when pressed to check lamp.

1-28.3.3.2 MAIN LIGHTS Circuit Breaker. Applies power to and provides overload protection for shelter main lighting system.

1-28.3.3.3 CURRENT Meter. Shows current of ac input power.

1-28.3.3.4 MAIN POWER Circuit Breaker. Applies main power to shelter and protects shelter and power source from current overload.

1-28.3.3.5 VOLTAGE Meter. Shows voltage of ac input power. During normal operation reading should be 103 to 127 Vac.

1-28.3.3.6 FREQUENCY Meter. Shows frequency of input power. During normal operation reading should be between 58 and 62 Hz.

1-28.3.3.7 CONTROL Circuit Breaker. Protects ac control circuit. Trips off and displays white band when control circuit is overloaded. Must be reset before any other circuit breakers can be set to on.

1-28.4 Regulator/Battery Charger. The regulator/battery charger provides the prime ac voltage to the dc bus in each circuit switch shelter and has a nominal value of 26.5 Vdc and an absolute voltage swing from 21 to 31 Vdc. The prime ac input voltage serves as the power source. The regulator/battery charger provides power to all of the loads connected to the dc bus.

When the prime ac power source is available, the regulator/battery charger also charges the battery bank. The battery charging process is concurrent with the furnishing of normal load power to the dc bus. During normal operation (prime power available), the regulator/battery charger provides a suitable amount of float charge current to the batteries. Provisions are made to reduce charging current to prevent damage to the batteries in the event a battery box over temperature condition is detected.

The regulator/battery charger is capable of fully charging depleted batteries within a period not exceeding 24 hours. During this period, the regulator/battery charger also provides power to the 26.5 Vdc loads. Protective circuitry is incorporated to ensure that the batteries are not damaged during the recharging cycle.

1-28.5 Battery Bank. The battery banks used in each shelter have the capacity to maintain dc operation of the critical loads for up to 10 minutes. The battery banks consist of pairs of batteries in a series configuration. Manual switching is not required to employ the battery bank as the power source in the event of ac failure. The voltage range of the series pair is 25 Vdc at full charge to 21 Vdc at the end of a discharge cycle.

The total number of battery pairs is consistent with the requirements of the shelter. Battery charging is provided by the regulator/battery charger. Protection circuitry is provided to isolate the battery bank from the dc bus when a fault harmful to battery bank occurs.

Maintenance considerations of the battery compartment include:

- Accessibility to the battery compartment for adding water to the batteries
- Accessibility to the battery compartment for removing and replacing batteries
- A circuit breaker is provided for the battery pair to electrically disconnect the battery pair from any other voltage source.

1-28.6 Main DC Bus. The power distribution system provides power for directly powered 26.5 Vdc loads. Normally, the bus provides a transmission medium between the regulator/battery charger and dc related loads. During emergency operation, the bus interfaces the battery bank and dc related loads. During battery charging, the bus interfaces the regulator/battery charger and the battery bank. The battery bank electrically floats on the bus.

1-28.7 Power Distribution Panel. The power distribution system provides the branch circuit breakers necessary for distribution of voltages within the shelter (fig. 1-34). The diagram identifies the major elements of the power distribution panel, including circuit breakers for the branch loads. The power distribution panel includes the following major components:

1-28.7.1 Power Processor Circuit Breaker. The power processor manual reset circuit breakers control the ac and dc power processors. They trip automatically if the dc bus voltage drops below 21 Vdc.

1-28.7.2 DC/AC Inverter Circuit Breakers. Where applicable, circuit breakers are provided to control the power to the dc/ac inverters. They trip automatically if the dc bus voltage drops below 21 Vdc.

1-28.7.3 DC Bus Circuit Breakers. Circuit breakers are provided to control loads which are powered directly from the 26.5 Vdc bus. They have the same operating characteristics as described above.

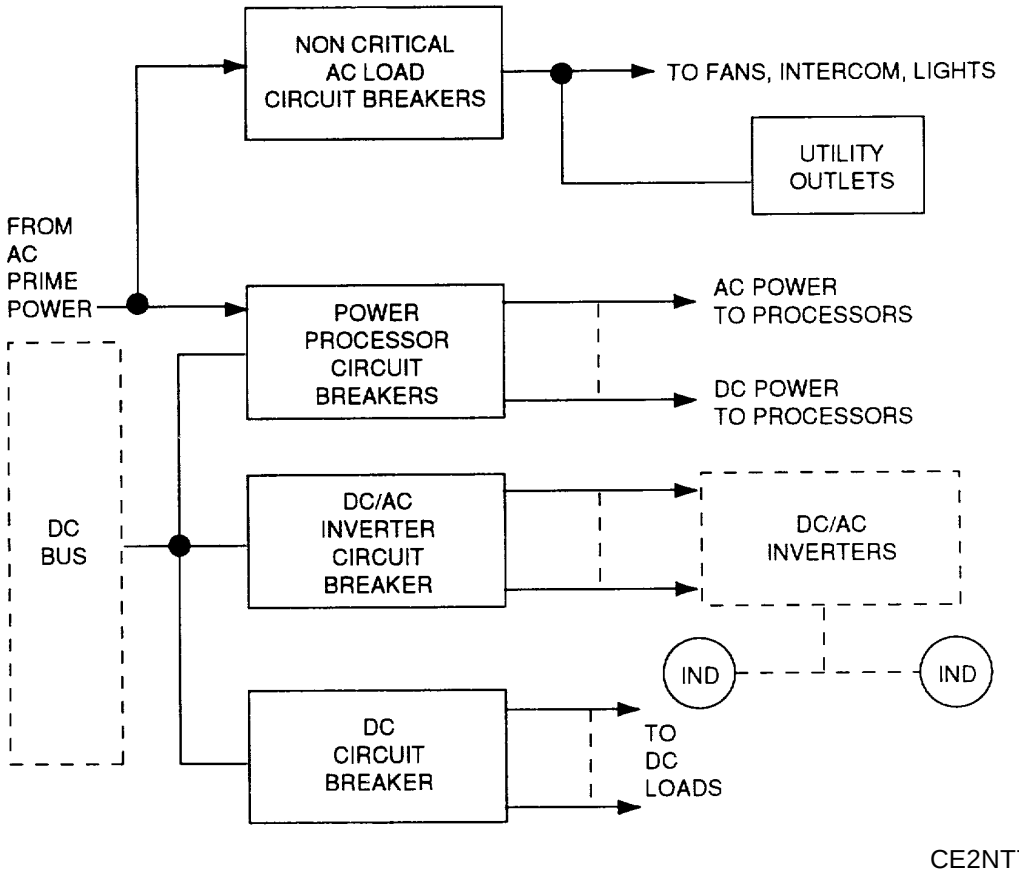


Figure 1-34. Power Distribution Panel Block Diagram

1-28.7.4 AC Load Circuit Breakers. Circuit breakers are provided to control non-critical loads which are powered directly from the prime ac power source.

1-28.7.5 Utility Outlets. Two duplex utility outlets are provided. These outlets accommodate 20-ampere loads.

1-28.8 DC/AC Inverters. DC/AC inverters are provided as a major element of the power subsystem. They provide a source of ac voltage to critical loads which must operate from an ac power source. The dc/ac inverter provides full operation when operating from a steady dc power source of +26.5 Vdc. The design of the dc/ac inverter prevents an overload or short circuit condition from causing permanent damage to the inverter.

1-28.9 Power Processor. The power processors provide secondary sources of power to loads requiring dc voltages other than that supplied by the dc bus. They have an input capacity of 115/208 Vac, 60 Hz, or 28 Vdc.

The input circuitry of the power processors uses a precedence technique when selecting input voltage. The precedence of the prime ac voltage, when present in the shelter, is employed in powering the power processors. In the absence of prime ac power, or during degradation of this power input source, the power processors automatically switch to 28 Vdc main bus without degradation to the regulated output voltages.

1-28.10 CPG Power Supplies. The CPG power supplies are dc/dc converters, that provide a +5 Vdc ± 5% secondary power source required by the two CPUs in the CPG, operating on +26.5 Vdc. The CPUs are protected from overvoltage or overcurrent damage by the incorporation of a crowbar circuit in the design, reducing the output towards zero, and trips on a (minimum) 5-microsecond pulse greater than or equal to 100 ma at 6.5 Vdc.

1-29 CONFERENCING.

There are four five-party bridges (conference bridge units) connected to TDSG 1 through CVSDs. Each five-party bridge has five four-wire ports which connect to the TDSG through the CVSDs (fig. 1-35).

Conferences of size between six and 14 parties are formed by interconnecting the five-party bridges through the TDSG (table 1-4).

The possible connections are defined in the following table. Each five-party conference bridge is capable of handling secure and non-secure conferences independently of the secure/non-secure nature of any other conference call in progress.

Table 1-4. Conferencing Interconnection to Form Larger Conferences

No. 5-Party Conference Bridges Interconnected	Conference Size Maximum
1	5
2	8
3	11
4	14

1-30 DIGITAL SWITCHING EQUIPMENT.

1-30.1 General. This listing provides a functional description of the following digital switching components:

- Time division matrix
- Switch multiplexer/demultiplexer
- Line driver interface
- Digital scanner
- Fault collector
- Diphase loop modem-A
- Group Modems
- Trunk Signaling buffer
- DIBTS signaling buffer
- Loop multiplexer/demultiplexer
- Transmission group module
- Remote signaling buffer controller multiplexer/demultiplexer
- Group multiplexer/demultiplexer
- Digital signal generator
- Digital receiver
- Essential user bypass
- Conference bridges
- Routing signaling buffer/data adapter.

Digital encryption and decryption is provided by the COMSEC equipment.

1-30.2 Time Division Matrix (TDMX).

1-30.2.1 General. The TDMX performs the digital switching of subscribers. These subscribers have been multiplexed into 64-channel data streams by the switch multiplexers. The calls are routed by reading the desired output data bit out of the data memory and placing it into the time slots of another subscriber. The time division matrix consists of a group of 15 TDMMs and two DSGs (fig. 1-36).

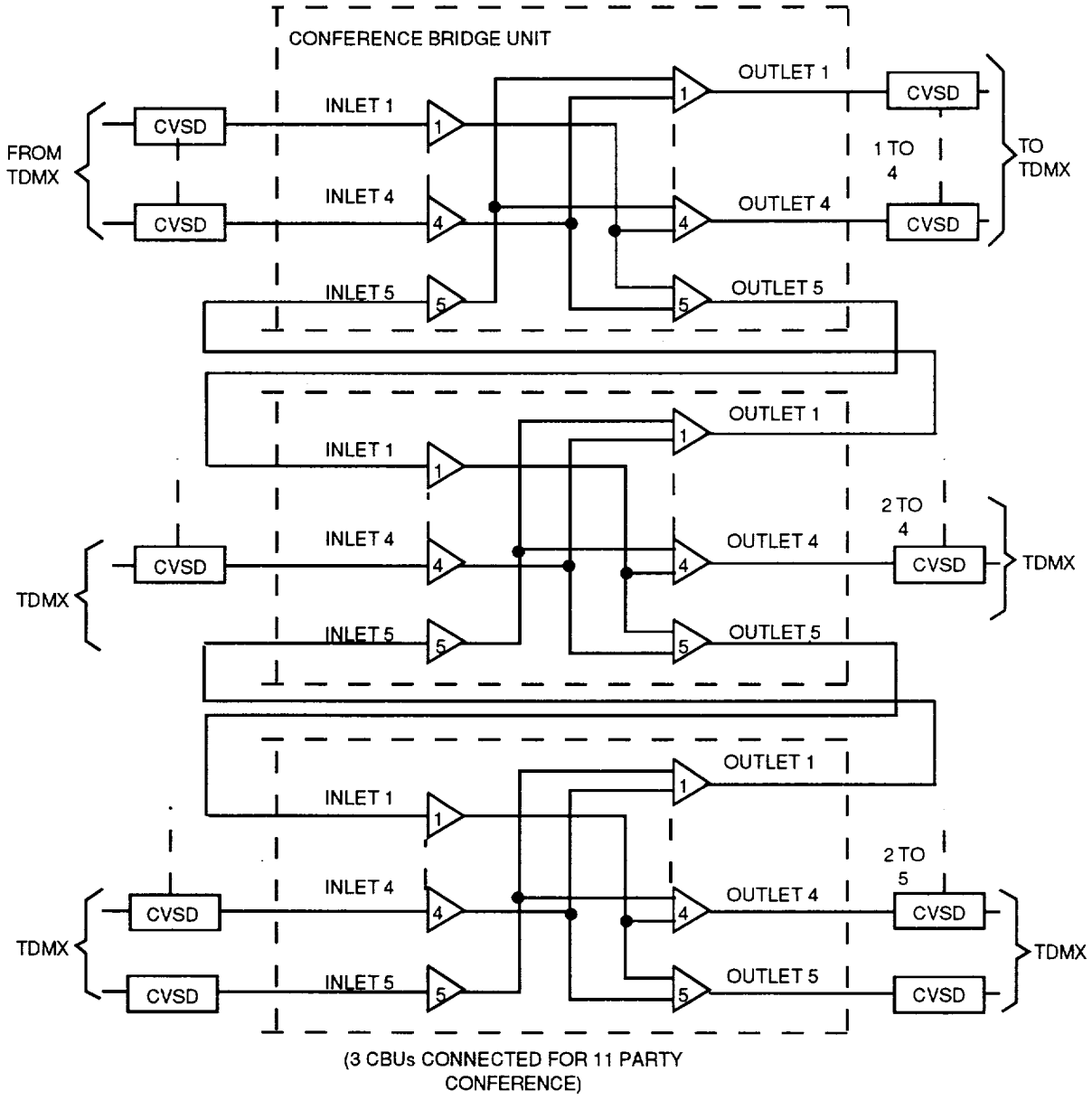


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Figure 1-35. Conferencing Functional Block Diagram

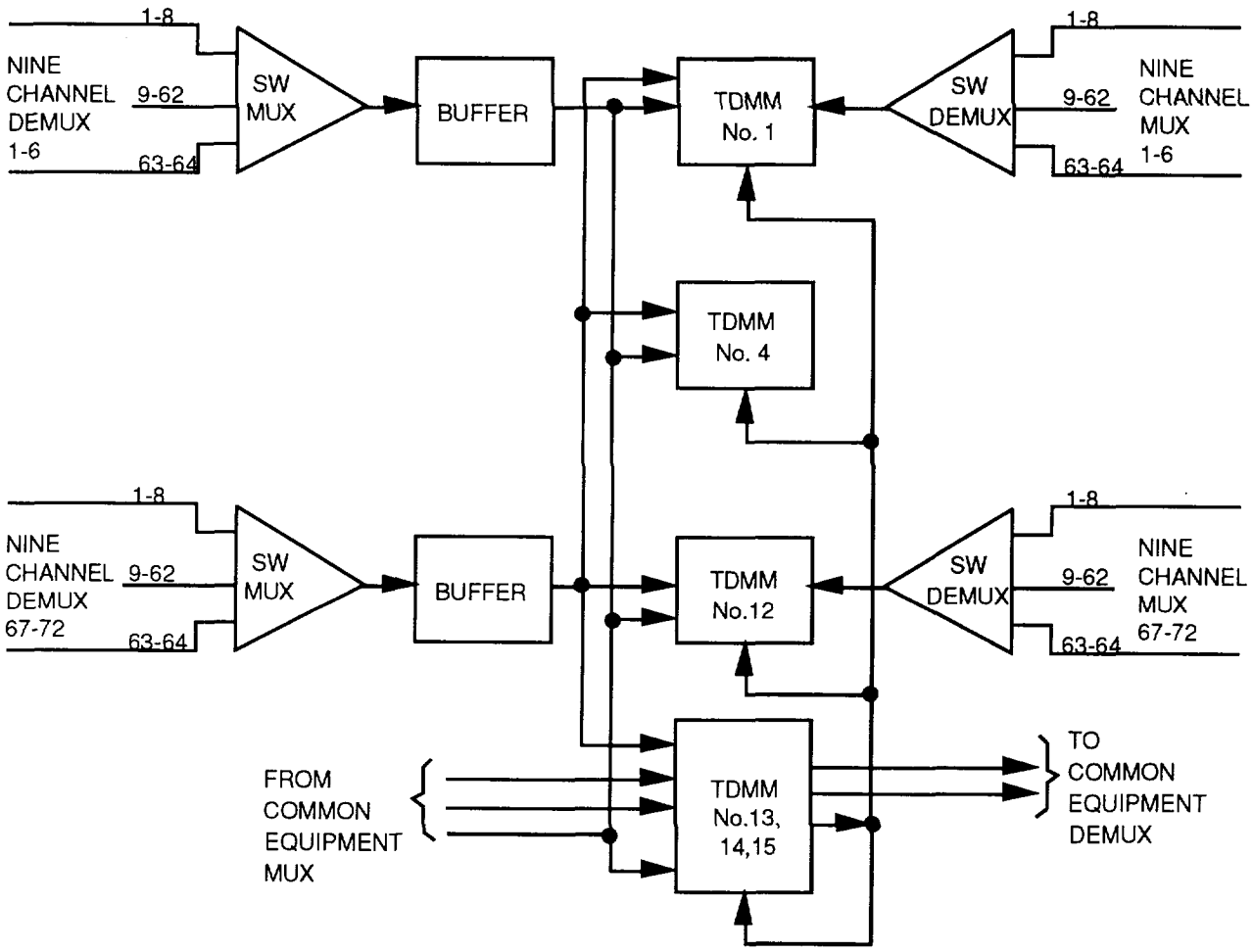

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Figure 1-36. Time Division Matrix Design

Each TDMM provides access through the switching network for 64 four-wire terminations. When TDMX #2 and #3 are employed, the spare memory and memory #5 are not used. Each TDMM within a given switch is assigned a binary number or bit select address. For a listing of TDMM assignments refer to table 1-5.

Within the TDMM, each of the subscriber addresses are defined as location addresses. The TDMM, when addressed by the processor, includes the bit select address and the location address. The memory address field is a 15-bit field consisting of five bits for the select address, six bits for the location address, and four bits of parity.

The TDMM performs the time division switching of multiplexed data streams originating at the switch multiplexers or DSGs. Each TDMM contains a 64 x 17 bit storage area for address location bits. Each TDMM contains all the logic necessary to interface with the switching controller group, and interpret the connection and control commands from the processor to perform the time division switching and memory check functions.

Table 1-5. TDMM Assignments

Binary (BS)	Devices
1	TDMM 1
2	TDMM 2
3	TDMM 3
4	TDMM 4
5	TDMM 5
6	TDMM 6
7	TDMM 7
8	TDMM 8
9	TDMM 9
10	TDMM 10
11	TDMM 11
12	TDMM 12
13	TDMM 13
14	TDMM 14
15	TDMM 15
16	DSG

TDMMs 1 through 12 are part of the MTDMF cards. Each MTDMF card includes a TDMM, SWMUX, SWDMX, six NCHMX/DMX, and the linedriver interface to the other MTDMF cards. The entire TDMF card is used for TDMMs 1 through 12. Part of the TDMF card is used for TDMMs 13 to 15.

1-30.2.2 TDMX Operation. A half connection can be made from bit select number 3, address location number 2 (subscriber No. 131) to bit select number 1, address location number 1 (subscriber No. 2) (fig. 1-37). Each group of 64 subscribers is multiplexed by the switch multiplexer into a single 64-channel 2.048-mb/s digital data stream. The data stream from each switch multiplexer is passed to every TDMM where the 64 data bit positions, one for each subscriber, are stored in the data memory at the appropriate bit select location.

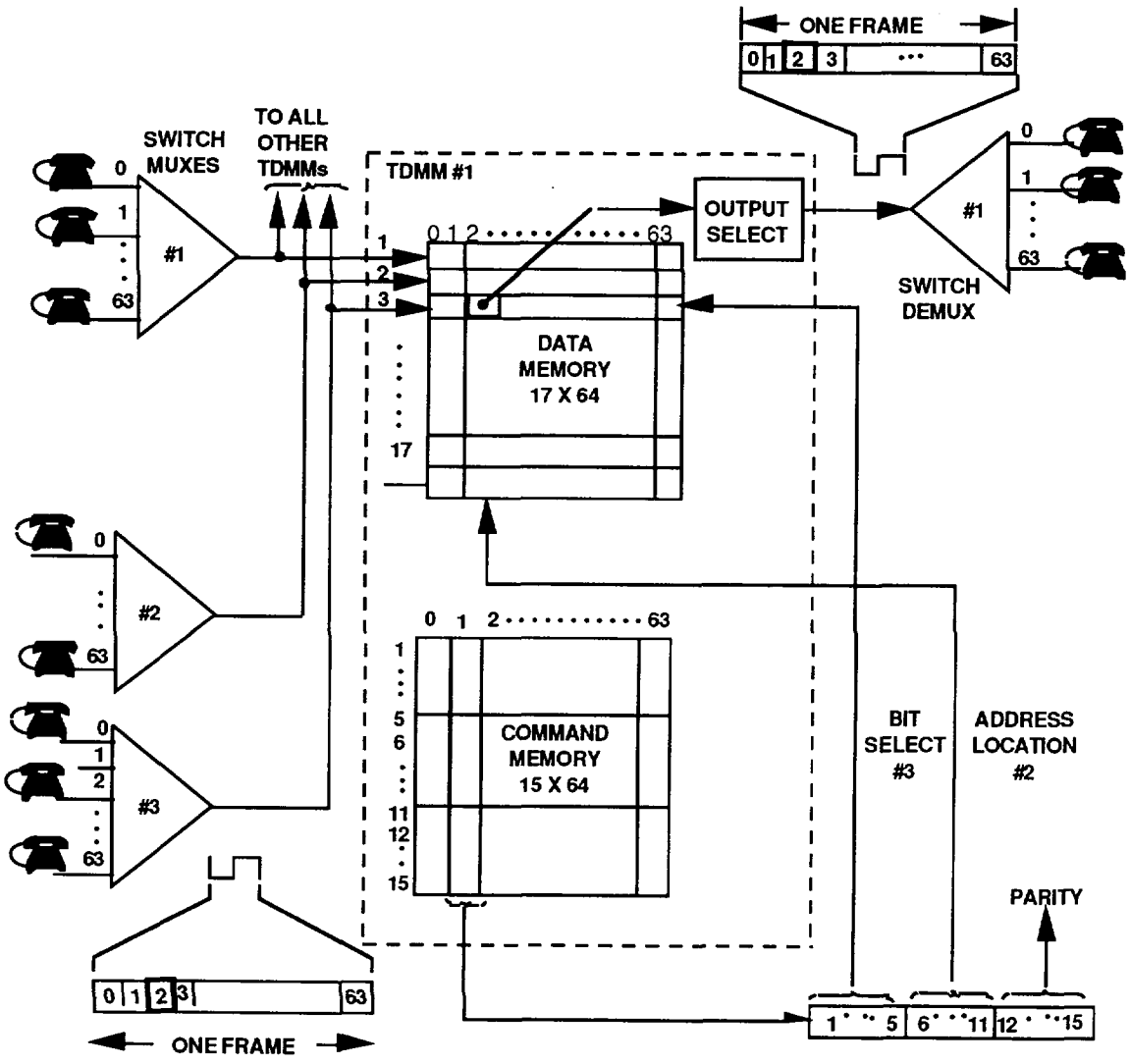
A fully populated circuit card contains 15 TDMMs, each contains a 17 x 64 data memory. All data memories are identical and contain an input data bit from each subscriber.

In addition to a maximum of 15 data streams from the switch multiplexers, there is a 64-channel data stream from the DSG. The DSG output data stream is passed to every TDMM in the circuit switch.

The half-connection command from the processor designates the originator's address as the recipient of the call.

The TDMM recognizing itself as the recipient, stores the originator address in the command memory at the recipient location. In the example, the originator address (bit select #3, address location #2) is stored in the command memory of TDMM #1 (bit select #1) at location #1 (address location #1). If this were a full connect command, bit select #1 address location #1 would be stored in the command memory of TDMM 3 at location #2.

The command memory is a 15 x 64 memory. The 64 locations in the command memory are read out synchronously to the output selector. For instance: the address location #1 to the command memory is read out and then violated with the parity bits. The bit select address stored determines the row in the data memory to be accessed, and the location address stored determines the column in the data memory. The data bit at the intersection of these two addresses is output in the time slot 1 (location #1) to the switch demux.



HALF CONNECTION FROM BIT SELECT #3, ADDRESS LOCATION #2 (ORIGINATOR)
TO BIT SELECT #1, ADDRESS LOCATION #1 (RECIPIENT)

CE2NT733

Figure 1-37. TDMX Operation: Half-Connection from Bit Select #3, Address Location #2 (Originator) to Bit Select #1, Address Location #1 (Recipient)

The above process is repeated for all 64 locations. The switch demux decombines the 64-channel bit stream into 64 individual channels. The data bit at location #1 is then output to subscriber #2, enabling subscriber #2 to listen to subscriber 131.

1-30.2.3 Processor Interface. The TDMX interfaces with the central processor through the matrix controller in the SCG. Control of the TDMX by software is by means of a two-word command. It contains the recipient and originator addresses and the specific command. The TDMX responds to each command by returning a status word to the processor.

1-30.2.4 Hardware Description. TDMX storage is divided into two sections (refer to FO-2, TM 11 -5805-78612-3). The data memory is a 64-word x 17-bit area assigned for the storage of subscriber data bits and the output bits from two digital generators. The storage area is a 64-word x 15-bit area assigned for the storage of relocation address data. The address data field is divided into a five-bit data select address, a six-bit data location address, and a four-bit address parity field.

Inputs to the address storage area are from the SCG interface while the data storage area receives inputs through a data bus which requires bipolar buffer circuitry. Both storage areas have memory address registers: they receive their inputs from an address select switch. The select switch determines if a relocation address or the channel counter output will be used to access a memory location.

The proper output data bit is selected in accordance with the relocation address given to the memory by the central processor. During each bit period, data storage memory is accessed by the six-bit data location address.

The resulting 17-bit output word coming from the memory appears at the input to a bit select switch. It then selects the proper output bit by means of the five-bit select address.

A data source select switch is used to output this bit to the switch demultiplexer (unless the processor has sent a select alternate data source command). If the processor has sent a select alternate data source command, the spare memory output will be selected. If no location address has been stored for a particular channel bit period, the memory will output a ONE. The absence of a location address in the memory is defined as the presence of all ONEs.

Each TDMM performs several modes of self-checking. A brief description of each mode is provided below.

1-30.2.4.1 Input Address Parity Check. When a command is sent from the matrix controller to the TDMM, the memory checks the parity of both the A and B input address contained in the 40-bit command word. When the parity fault is found, a fault line is activated and the command inhibited.

1-30.2.4.2 Stored Address Parity Check. The parity check of each of the 64 locations in the address storage area is checked during each frame period. If one location is found to have incorrect parity, a fault line is activated.

1-30.2.4.3 Time Slot Counter Check. Each memory contains logic. It shows a comparison between the counter output and either A or B addresses sent as part of the 40-bit SCG command word. This operation is checked by maintaining a count of comparison indications during each frame period. If either the A or B logic gives more than one comparison indication during a single frame period, a fault line is activated.

1-30.2.4.4 Output Data Select Check. Each TDMM contains logic which selects one of the 17 bits read from the data storage area. It compares the output bit with the output bit from another TDMM. If a fault is detected, a fault line will be activated.

1-30.2.4.5 Data Memory Check. During each time slot, the parity (even) of the 17 data bits stored in the data storage area is checked. This parity bit is then compared with the parity bit of two other memories. A memory signals a fault only if it finds fault. If a fault is detected, a fault line is activated.

1-30.2.4.6 Test Logic Verification. The logic which performs time slot counter, output data select, and data field parity checks also contains logic which verifies the proper operation of the check logic itself (fig. 1-38). When the processor sends a test command, it results in a check of the BITE logic for the address memory. When the command is received by the TDMM, an error is generated. It is sent to the TDMM fault detection circuitry.

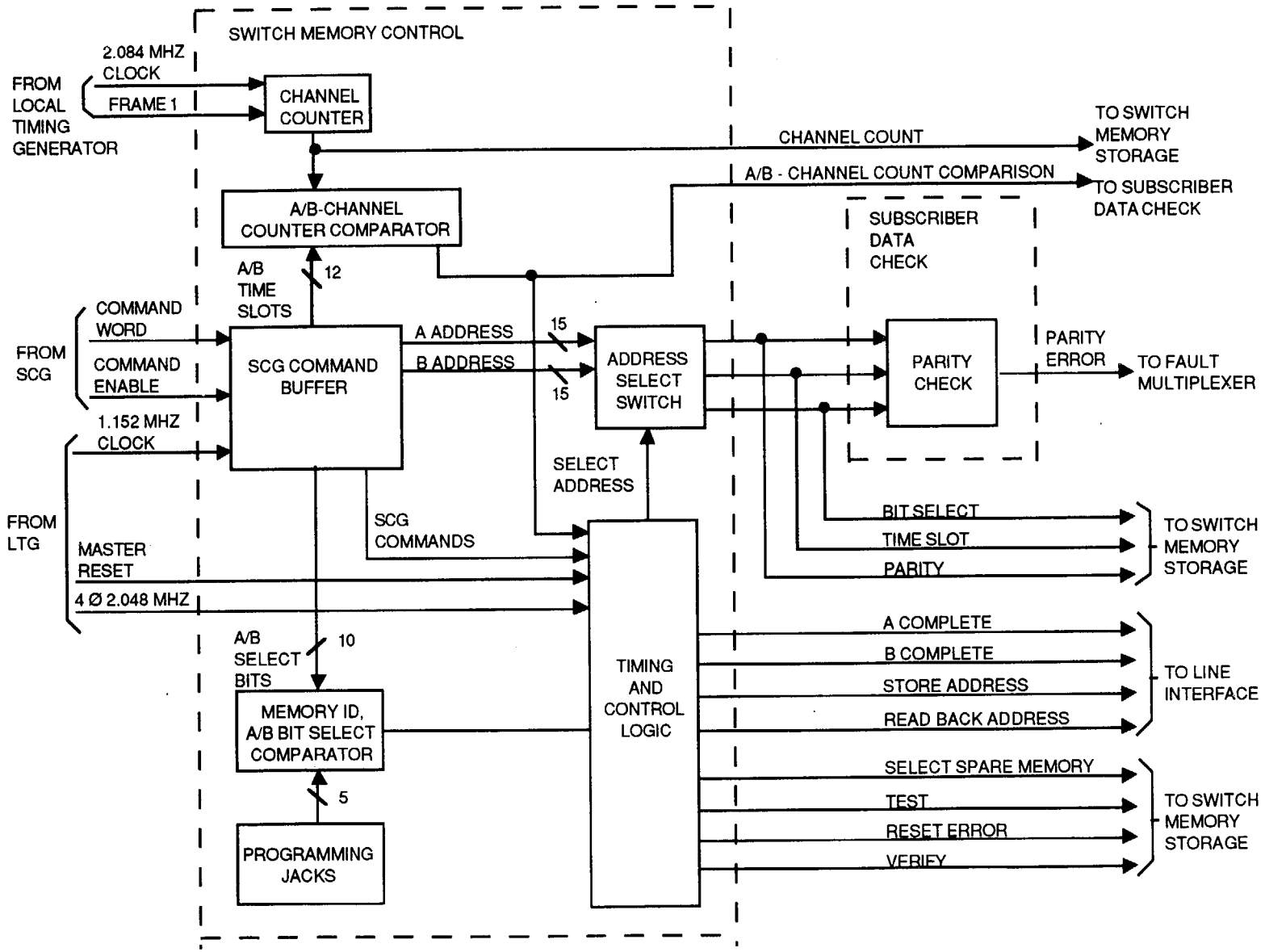


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Figure 1-38. TDMM Timing and Control Block Diagram

A four-phase 2.048 MHz clock is used for internal timing along with a subchannel framing pulse for sync. A channel counter provides the addressing of data and address storage area. The timing and control logic determine the operations to be performed (based on commands arriving from the SCG).

1-30.3 Switch Multiplexer/Demultiplexer.

NOTE

Rates that are given below are for switch rate of 32 kHz. Rates are one-half those shown when switch is set for 16 kHz. CC circuit switch rate is usually 16 kHz.

1-30.3.1 Switch Multiplexer. The switch multiplexer combines 64 32-kHz digital data streams into a 64 channel, 2.048-MHz multiplexed data stream. This is input to all time division memory modules (fig. 1-39).

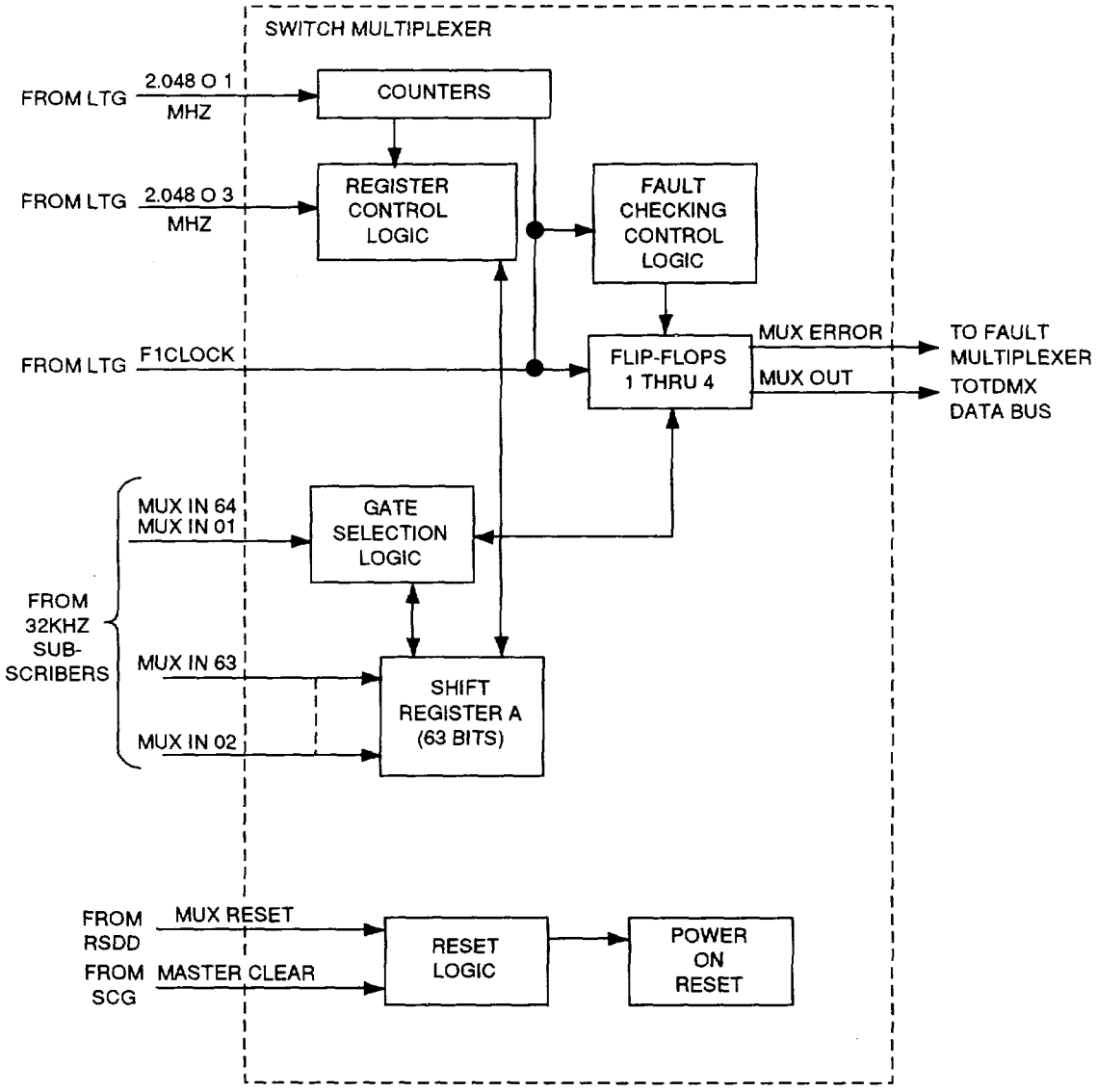

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Figure 1-39. Switch Multiplexer Block Diagram (Part of TDMF Card)

The multiplexing technique uses a parallel-in/serial-out shift register (register A). The 64 data streams at 32 kHz are sampled and their contents stored in the 64 bits of register A. Data stream no. 1 (corresponding to channel 0) is stored in bit 1 of register A. Data stream 64 (corresponding to channel 63) is stored in bit 64 of register A. The data stored in bit 1 of register A immediately appears at the output of the multiplexer. The 2.048-MHz clock then shifts the contents of the other 63 bits into bit position 1, thus creating a 2.048-MHz data stream with 64 channels.

The channel counter maintains a count of the previous time slot in the multiplexed data stream. It determines when to clock the next 64 bits into register A. The register control logic uses the 2.048-MHz clock, channel counter output and the subchannel framing pulse F1. They control the shift/load operation of register A.

Logic to check the operation of the multiplexer is included on the switch multiplexer. When the 64 bits are stored in parallel in register A, channel 63 is also stored in flip-flop one. The 64 bits are then shifted serially through the register. When channel 63 is clocked into position two of register JA, it is compared with the bit stored in flip-flop one. If the bits do not compare, a fault line to the fault mux is activated and the multiplexer is inhibited.

More BITE is provided by the gate selection logic. Two counters are provided; one controls the multiplexing operation while the other controls the fault checking operation.

A line from the special devices resets the fault status bit in the multiplexer. The multiplexer receives a master reset line in addition to having a power-on reset circuit located on the PWB. These two functions clear the contents of the fault status flip-flops when any of the following events occurs:

- A master clear pulse is sent by the processor
- The circuit card is inserted into a powered up nest
- Power is applied to the circuit card while in the nest.

1-30.3.2 Switch Demultiplexer. The switch demultiplexer accepts the 2.048-MHz output of a TDMM. It decodes it to 64 individual 32-kHz digital data streams. The switch demultiplexer utilizes serial-in/parallel-out shift registers (fig. 1-40).

The 64-channel multiplexed data stream from the TDMX is sampled and clocked serially into registers A and B. The 32-bit register A acts as a delay, to provide the proper sync for strobing data into register C. The outputs of register C are then demultiplexed 32-kHz digital data streams.

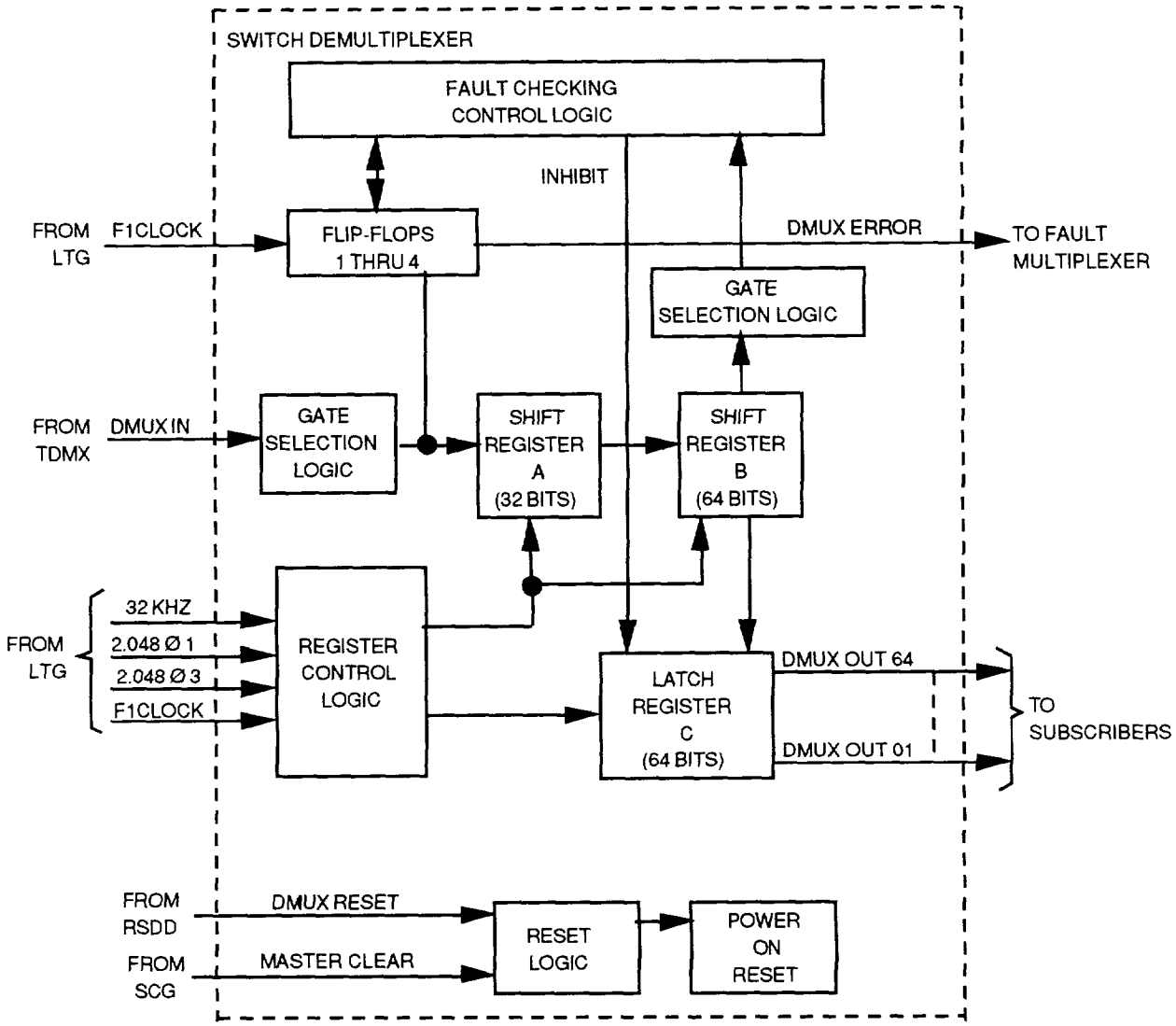
Fault checking logic is employed to detect any failure in the serial-to-parallel conversion. A line from the special devices resets the fault status bit in the demultiplexer.

The demultiplexer also receives a master reset line in addition to having a power-on reset circuit located on the circuit card. These two functions clear the contents of register C and the fault status flip-flops when:

- A master clear pulse is sent by the processor
- The circuit card is inserted into a powered up nest
- Power is applied to the circuit while in a nest.

1-30.4 Line Driver Interface (LDI). The LDI circuit performs logic level conversion between transistor-transistor logic (TTL) and low level, balanced bipolar logic for various circuits in the circuit switch. The TTL levels are used within a cabinet; the balanced lines are used to transmit signals over the longer distances between cabinets. The LDI provides the necessary line driving and receiving capability for these interfaces. Up to 100 feet of unterminated, balanced twisted pair of No. 28 to 30 AWG with a characteristic impedance of 80 to 120 ohms and a maximum capacitance of 15 picofarads per foot can be driven by the LDI.

The electrical interfaces of the LDI are as given in table 1-6. Also, refer to figure 1-41.

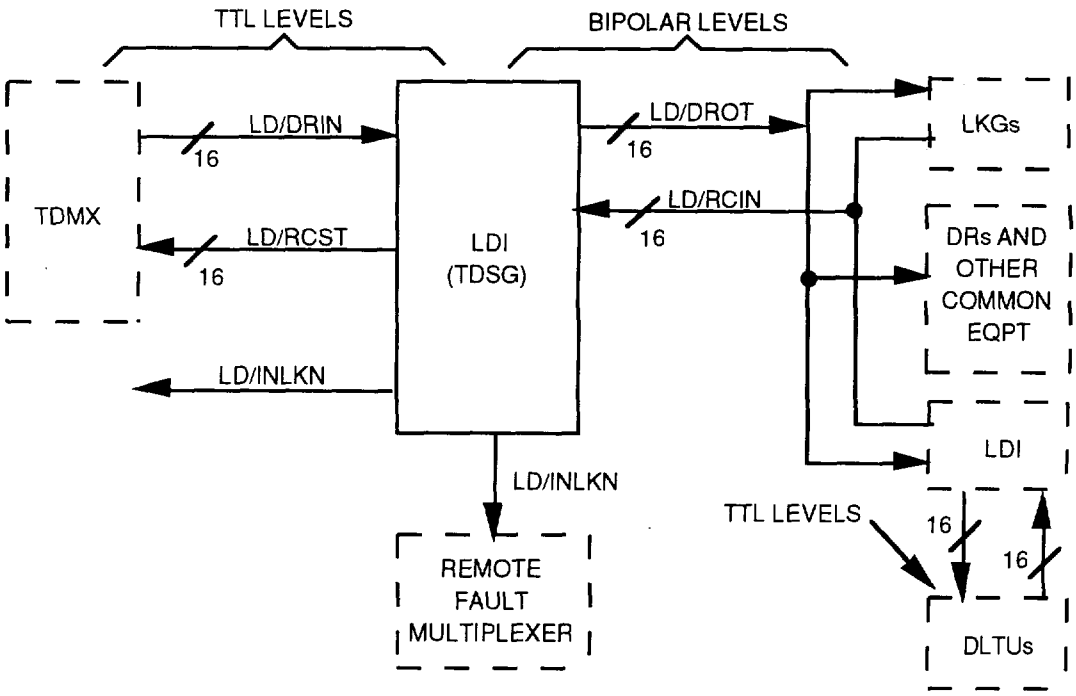


CE2NT736

Figure 1-40. Switch Demultiplexer Block Diagram (Part of TDMF Card)

Table 1-6. Electrical Interface

SIGNAL LINE/NAME	LDI/DEVICE INTERFACE	DEFINITION
LD/DRIN	TDSG	TTL input to LDI
LD/DROT	LKG or DR equipment	Bipolar driver output
LD/RCIN	LKG or DR equipment	Bipolar receiver output
LD/RCST	TDSG	TTL output from LDI
LD/INLKN	Remote fault mux	Card present signal line
POWER	Voltage buses	



CE2NT737

Figure 1-41. Line Driver Interface Block Diagram

The LDI operates with TRUE and FALSE logic levels to accomplish bipolar to TTL conversion. TRUE and FALSE logic levels are derived by a differential voltage of at least 0.3 Volts but not more than 3 Volts at the LDI output. The sign of the differential voltage indicates the logic sense (plus = TRUE, minus = FALSE) of the signal. Signal swings on each line of the pair are balanced within 10 percent of each other. The true (one) signal (or more positive voltage) is provided on the higher numbered connector pin relative to the corresponding lower numbered pin. The TTL true (one) is 0.0 to 0.4 Volts and the TTL false (zero) is 2.4 to 5.5 Volts. The LDI operates at either 16 or 32 kb/s data rate.

1-30.5 Digital Scanner (DS). The DS performs the sequential search of all TDMX switched lines and trunks in order to monitor their supervision status. Once a change in the status is detected, information describing the new status state is forwarded to the processor via the SCG unless it is a change to a no-code status which is noted internally but not transmitted.

The TDSG contains four DSs, each capable of monitoring 192 incoming channels for the presence of plain text supervisory signals. The DS is connected to the output of three switch multiplexers and scans three 64-channel time-multiplexed groups simultaneously.

The information signals that are detected are in the form of eight-bit permutable codewords and are transmitted to the switch processor via the SCG. The valid eight-bit codewords that are detected along with the reported binary code are given in table 1-7. The operation of the DS is as shown in figure 1-42. The DS block diagram is shown in (fig. 1-43).

Table 1-7. Valid Eight-Bit Code Words

SIGNAL	CODE WORD		BINARY CODE
Release	1111	1010	0001
Recall (Not used by software)	1100	0000	0010
Lock In	0000	0000	0011
Ring Acknowledge	1101	0100	0100
Ring Trip	1100	1010	0101
Conference/C-Key	0001	0001	0110
Seize/R-Key	1111	0110	0111
P-Key, Reply/Interrogate	1110	0010	1000

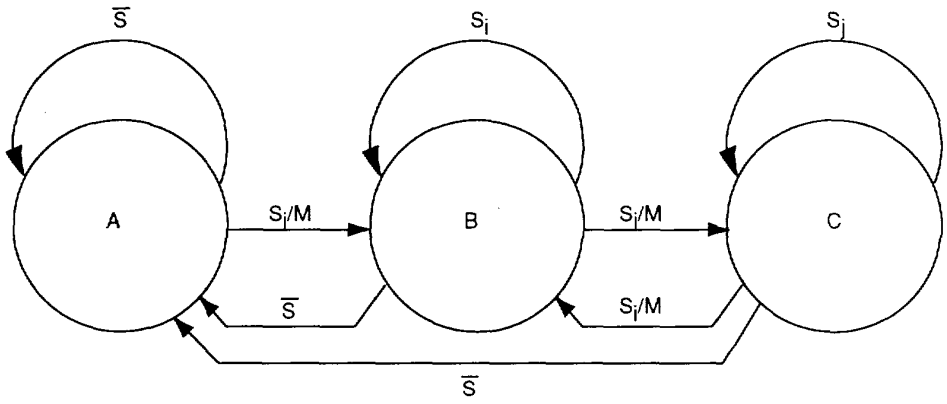


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Figure 1-42. Digital Scanner State Diagram

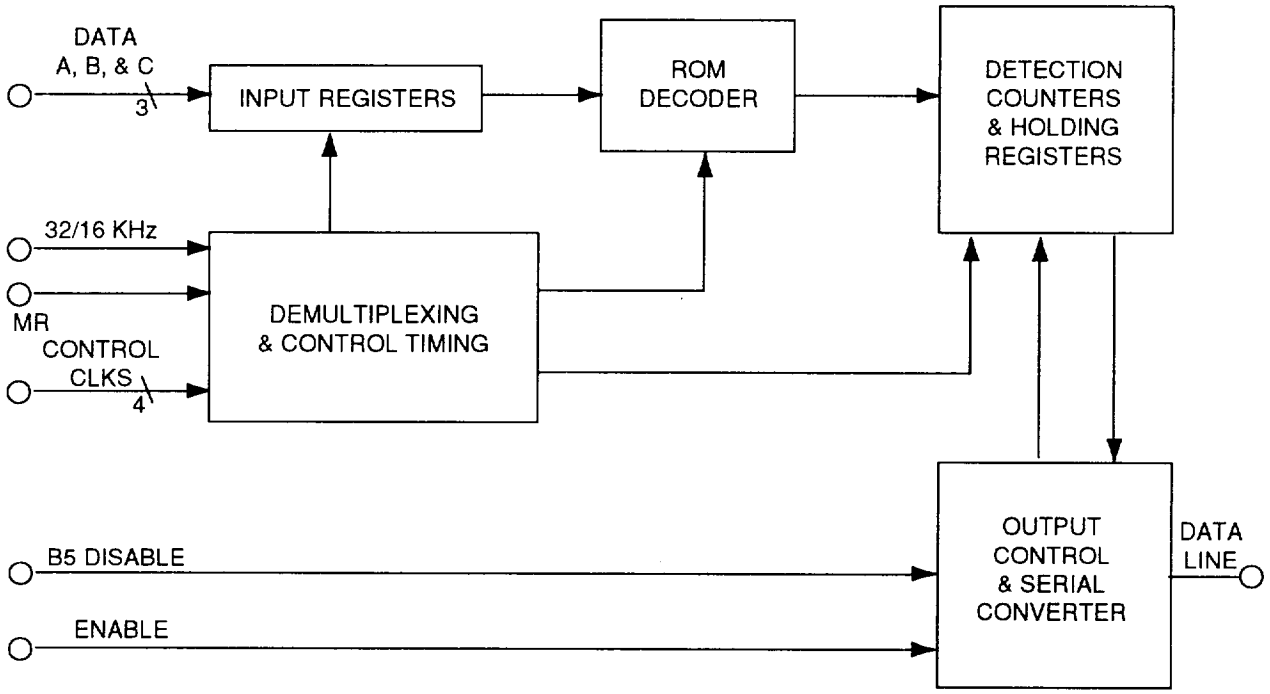

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Figure 1-43. Digital Scanner Block Diagram

The input registers accept three serial data streams from the switch multiplexers, perform a demultiplexing function to extract the single channel data, and format the data into eight-bit permutable codewords. Three parallel eight-bit words are generated for decoding.

The eight-bit words are sequentially applied to the address input of a read only memory (ROM). The word stored in memory and thus read out contains information as to (a) whether or not the eight-bit word is a valid codeword, (b) which code it is, and (c) which permutation it is in.

The detection counters and holding registers consist of 64 four-bit counters (one for each permutation of all eight valid codewords) and 64 four-bit holding registers (one for each input channel). The output from the ROM decoder addresses the proper counter and increments it when a valid codeword is input to the DS. When one of the counters exceeds nine, the current codeword is compared with the one in the holding register for the appropriate channel. If the current codeword represents a change of state from the previous codeword, it is stored in that channel holding register and a report is formatted for transmission to the processor.

After examining 16 codewords all the counters are reset and, if no detection is made, a no-code status is written into the holding register for that channel.

The output control and serial converter provides the interface timing and parallel-to-serial conversion necessary to transmit a detection report to the processor.

Clock and gating signals are generated in the demultiplexing and control timing to provide for the proper channel demultiplexing, codeword decoding, and codeword detection.

1-30.6 Diphase Loop Modem-A (DLPMA). The DLPMA provides the synchronous four-wire full-duplex data interface between individual digital subscribers and the TDMX (fig. 1-44). This loop modem, referred to performs the following operations:

- Transmits/receives conditioned diphase signals over 4 km of WF-16 field wire and WM-130 cable at a BER of one part per million (ppm) or less
- Modulates baseband signals from the LEN and demodulates the conditioned diphase signals
- Provides a dc phantom loop for remote powering of the DSVT or DNVT
- Detects the presence or absence of a carrier
- Performs the proper subscriber signaling function
- Recovers a clock from the received diphase signals to enable synchronous bit detection
- Reclocks the detected data bits into the loop multiplexer/demultiplexer using the switch clock.

The diphase loop modem consists of a modulator and a demodulator section. The modulator accepts baseband data at 16 kb/s and converts the baseband data to conditioned diphase data.

1-30.7 CVSD Modulation. Voice digitizing is performed by the complex delta modulation technique called Continuously Variable Slope Delta (CVSD) modulation (fig. 1-45). CVSD modulation provides for analog-to-digital and digital-to-analog conversion which allows analog voice subscribers to converse with digitized voice subscribers (as well as with other analog voice subscribers) over digital trunks.

The CVSD modulation technique is a method of digitizing voice signals into a single serial digital bit stream which consists of pulses of fixed amplitude and timing (the only variation being in the pattern of ONEs and ZEROs). The method depends upon the fact that when the input level to the CVSD encoder is increased, more runs of consecutive digits of the same polarity are produced at the digital output. The CVSD encoder operates by comparing the speech input with the feedback approximation from the loop integrator. The output of the analog comparator is a logic ONE if the speech input voltage is more than the approximation feedback voltage and a logic ZERO if it is less. The output of the analog comparator is sampled at the clock rate and three consecutive bits are stored in the shift register. The logic decoder circuit detects whether these three bits are all ONES or all ZEROs. If they are all ONEs or all ZEROs, a logic ONE is produced at the decoder output. The syllabic smoothing integrator smooths the decoder output pulses to produce the control voltage Vc. The pulse height modulator produces a pulse whose amplitude is a linear function of the control voltage Vc and whose positive or negative sense is a function of the bit stored in the first stage of the shift register. If a ONE is stored in the first stage, a positive gain is produced by the pulse height modulator, and conversely, a negative gain is produced if a ZERO is stored in the first stage of the shift register. The loop integrator produces the approximated speech input signal by integrating these height-modulated pulses.

As the RMS value of the speech input signal increases, a greater number of runs of three consecutive like digits is produced, which produces more ONES at the logic decoder output and, therefore, the control voltage Vc increases. This increases the peak-to-peak output voltage of the pulse height modulator and enables the feedback approximation to more accurately follow the input speech signal.

The CVSD decoder operates identically to the encoder and has identical characteristics except that it runs open loop and does not require the analog comparator. A low-pass filter is included at the output of the CVSD decoder to remove the quantizing noise and other frequency components above 4 kHz.

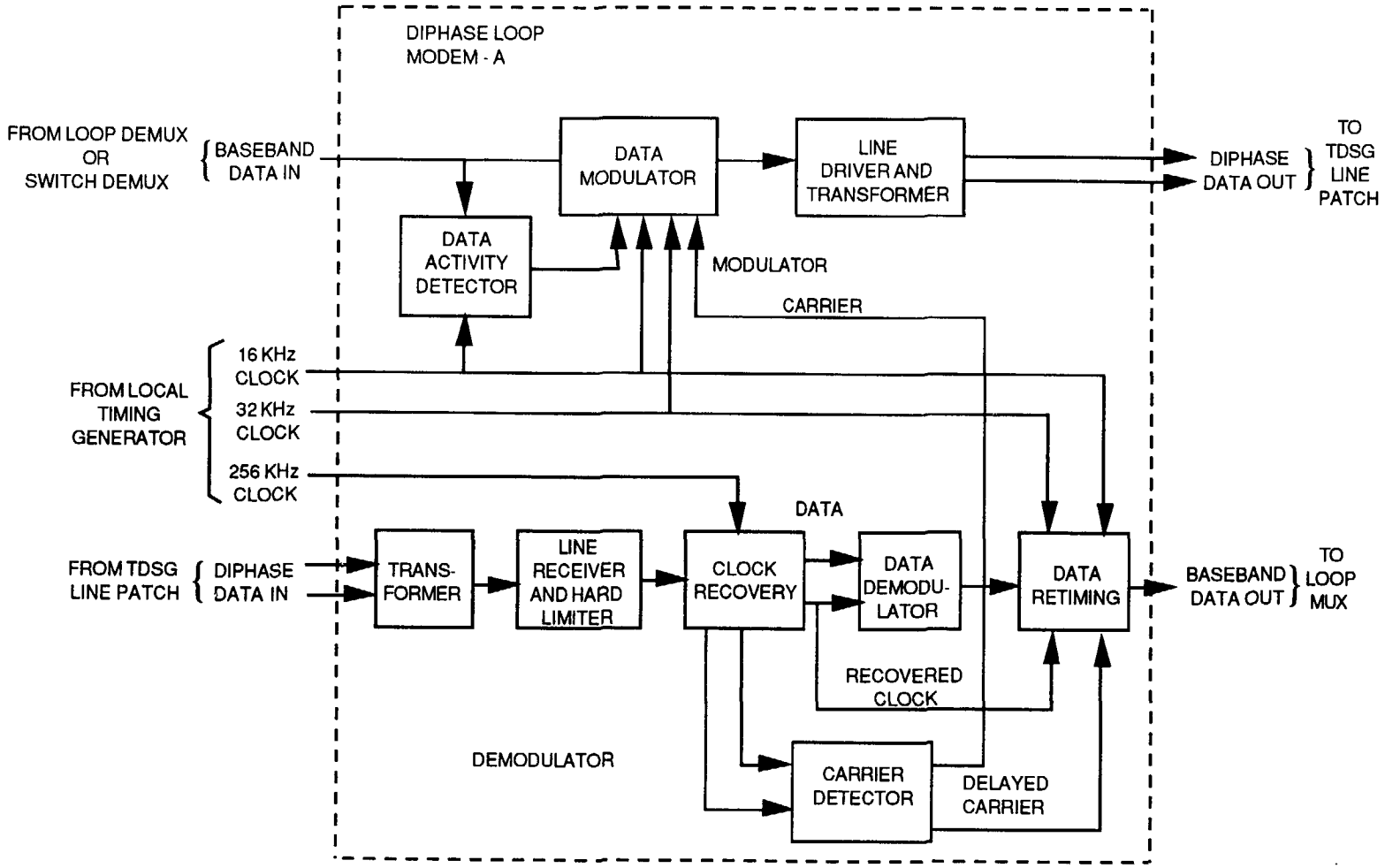

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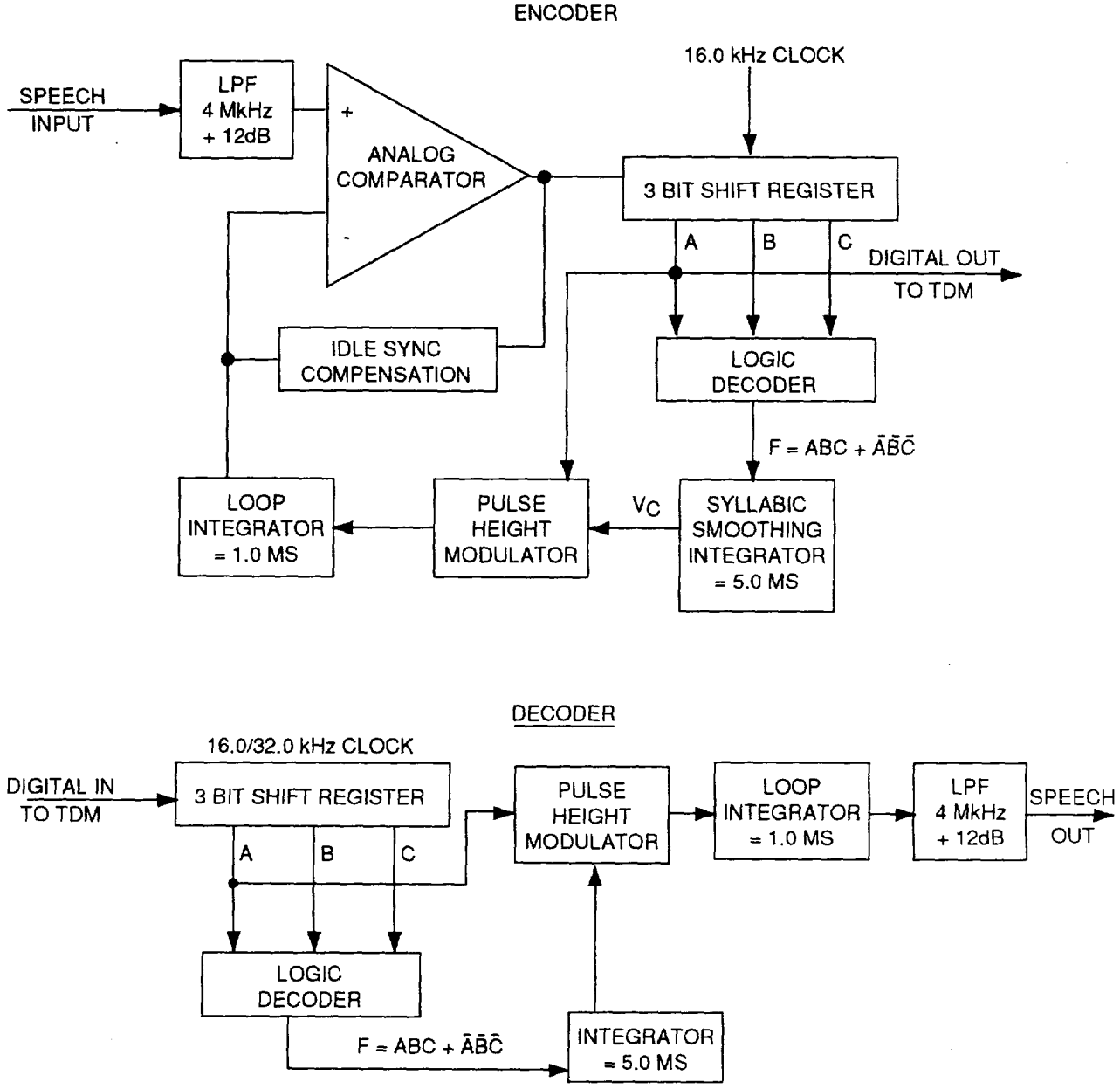
Figure 1-44. Diphase Loop Modem (Type A) - Block Diagram



CE2NT741

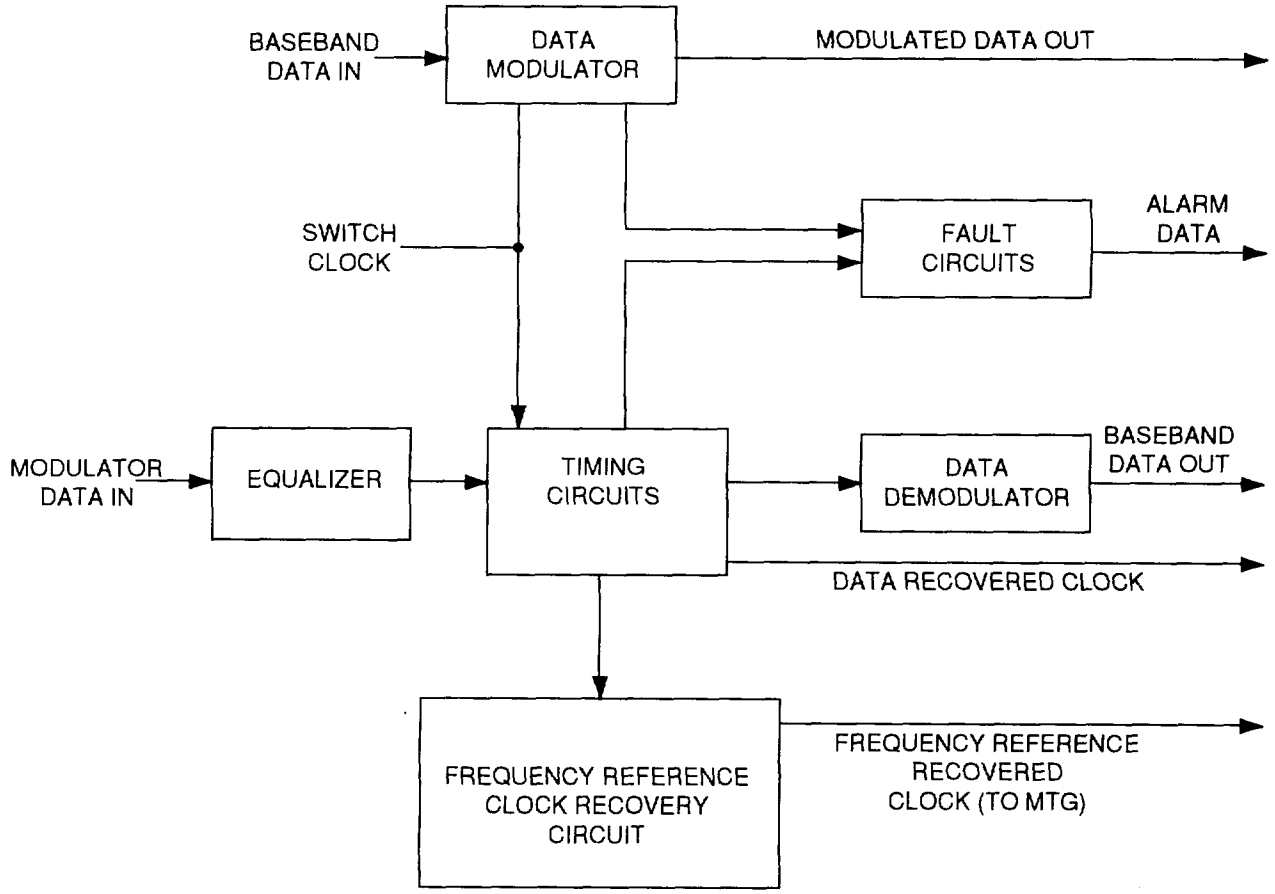
Figure 1-45. CVSD Block Diagram

1-30.8 Group Modems. The GM circuit card provides for two types of modulation: diphase and dipulse. Selection of modulation type is by processor controlled strapping (PCS). The GM receives two eight-bit words from the Special Devices Controller (SDC) that supplies strapping information for controlling the following functions: * Data Rate

- Modulation (Diphase or Dipulse)
- Cable Length
- Loop Back
- Modem Identification.

The GM consists of high-speed modulator/demodulator circuits, timing circuits, cable equalization circuits, frequency reference recovered clock circuits, and fault circuits (fig. 1-46). Provision is made for full-duplex transmission of synchronous digital data signals at all transmission group modularities from 4 1/2 to 144 channels between the CC circuit switch and external equipment (such as radios, multiplexers, and other MSE shelters).

The modulator and demodulator use two types of modulation: diphase and dipulse. Conditioned diphase is used on all direct coaxial cable links between a CC and (a) another CC, (b) a NC, LEN, SEN, RAU and LOS, and (c) any compatible multiplexer and radio components of the digital equipment family currently being designed. Dipulse modulation is used to interface with existing Army multichannel transmission equipment; e.g., the TD-754, TD-204, AN/GRC-144, and AN/GRC-143.



CE2NT742

Figure 1-46. Group Modem Functional Block Diagram

The GM provides a recovered received data clock to the GB in the transmission group module. In addition, a bit synchronous reference frequency recovered clock is made available from two selected DTGs for use by the MTG. The MTG, via the LTG, provide the modems with the clocks necessary to perform the modulator, demodulator, and recovered clock functions. The clock is derived from the Atomic Frequency Reference or from one of the two recovered clocks.

In the received circuits, the GM provides an equalizer for the one mile of cable and attenuators which can be set to simulate cable in one-quarter-mile increments.

The GM also provides cable length simulator attenuators in the transmit circuits for the dipulse-modulated modems. No attenuators are provided in the transmit circuits for diphase modulated modems.

The GM returns four status lines and a loopback indicator to the processor through the remote fault mux and fault controller. The four status alarms are:

- Modulator Data Alarm: indicates absence of transmit baseband activity
- Modulator Carrier Alarm: indicates absence of transmit carrier activity
- Demodulator Carrier/Recovered Clock Alarm: indicates excessive carrier noise and/or loss of recovered clock
- Demodulator Data Alarm: indicates absence of received baseband data activity.

For testing purposes, the GM has the capability to loopback; that is, connect output to input and pass data from modulator to demodulator. The group modem returns a status line indicating that the modem is operating in the loopback mode.

1-30.9 Trunk Signaling Buffer. The TSB, in conjunction with the SBC, provides for the common channel signaling (fig. 1-47). The TSB performs the encoding, decoding, data storage and message formatting necessary to allow signaling from one switch to another. The TSBs are packaged two per card. The CC standard database is populated with eight TSBs, although the card will work in any of the 20 signaling buffer locations.

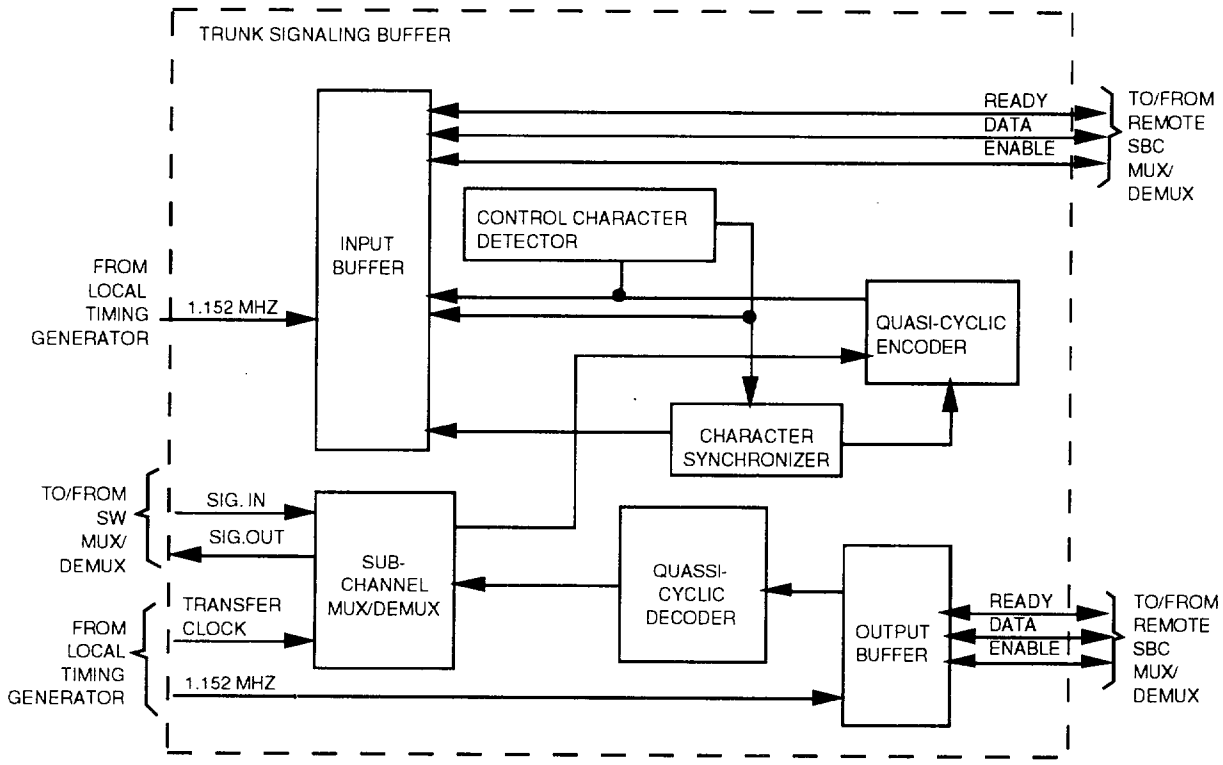
Each TSB consists of:

- Subchannel mux/demux
- Quasi-cyclic encoder and decoder
- Control character detector
- Character synchronizer
- Input and output message buffers.

1-30.9.1 Subchannel Mux/Demux. The subchannel mux/demux provides for the combination of 2/4 kb/s frame code and the 8/16-kb/s signaling data into one 16/32 kb/s outgoing channel. The multiplexed data stream will contain one 214 kb/s channel. The subchannel mux/demux also decombines the incoming 16/32-kb/s data in the opposite manner.

1-30.9.2 Quasi-Cyclic Encoder and Decoder. The quasi-cyclic encoder generates the quasi-cyclic (16, 8) code. The quasi-cyclic (16, 8) code is a block code. Each block contains eight information bits and eight redundancy bits for a total block length of 16 bits. This code is capable of correcting one or two errors anywhere within the 16-bit block.

The quasi-cyclic decoder detects errors by separating the received word into its data field and checking bit field components. The data field is re-encoded at the receiver using the same encoding process as described previously. The resulting bit field is added (module-two) to the received check bit field. The result, in the absence of transmission errors, will be an all-ZERO remainder. A non-ZERO remainder indicates the existence of bit errors in the received word and can be interpreted for the presence and location of one or two random errors.



CE2NT743

Figure 1-47. Trunk Signaling Buffer Block Diagram

1-32.9.3 Control Character Detector. The control character detector recognizes the start-of-message (SOM), end-of-message (EOM), and idle characters. It generates the necessary control signals for the proper gating of the incoming messages into the input buffer. In addition to detecting characters, the detector also checks the parity of all incoming characters. Any eight-bit character having even parity will be replaced by a parity error character.

1-32.9.4 Character Synchronizer. The character synchronizer accomplishes character sync by manipulating the character sync timing. It does this until it observes the detection of three consecutive idle characters by the control character detector. Once synchronized, the unit continues to monitor sync by examining the detector output. It does this for at least one idle or SOM character out of 100 incoming data characters. Failure to observe either one causes resynchronization. Status information will be transferred to the processor using the receive control word.

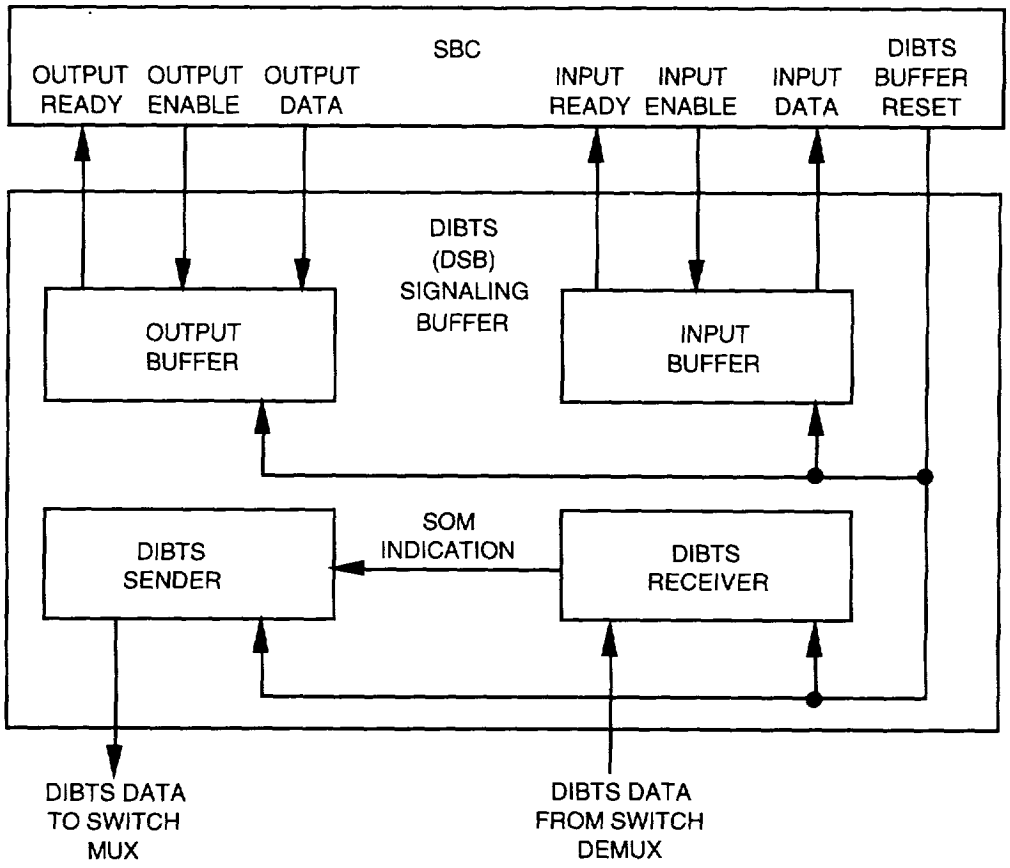
1-32.9.5 Input and Output Buffer. The input buffer uses the signals from the control character detector. It does this to effect the proper loading of signaling messages into a 64-character FIFO buffer. Their transmission to the processor through the SBC is then achieved. The input buffer initiates loading with each SOM and loads all characters up to and including the one following an EOM (message parity). If no EOM is observed within 32 characters (maximum message length) or a second SOM is observed, the buffer then terminates the message.

The output buffer contains a 64-character FIFO buffer similar to the input buffer. Whenever buffer space for 32 characters exists, the output buffer signals the SBC that it can accept data. When the buffer is empty, idle characters are output.

1-30.10 Digital In-Band Trunk Signaling Buffer. The digital in-band trunk signaling (DIBTS) buffer (DSB) provides a means of in-band signaling and supervision between a COMSEC parent switch and a COMSEC subordinate switch (fig. 1-48). The DSB provides for the transmission and reception of DIBTS data via the time division switching group (TDSG). It also provides for the exchange of this data with the circuit switch processor via the SBC. DIBTS buffers may be substituted for TSBs in any of the 20 signaling buffer locations. The DIBTS buffers are packaged two per card.

The DSB consists of four functional blocks as shown in figure 1-48. The output buffer and the DIBTS sender are involved in transmitting messages from the SBC to the switch MUX (ultimately the CPG). The DIBTS receiver and the input buffer are used in transmitting messages from the switch DEMUX to the SBC.

1-30.10.1 Output Buffer. Activating the SBC OUTPUT READY line indicates to the SBC that the output buffer is ready to receive an SBC message. Enable pulses are sent over the SBC output enable when the SBC message is ready to be transmitted. For each enable pulse one word is input to the output buffer over the SBC OUTPUT DATA line The SBC OUTPUT READY line is reset after the first enable pulse. This ensures that the output buffer is ready for the next message after the complete message has been read in.



CE2NT779

Figure 1-48. DIBTS Buffer Functional Block Diagram

1-30.10.2 DIBTS Sender. The DIBTS sender formats the SBC message received by the output buffer and transmits it to the switch MUX. If indicated by the control word, the DIBTS sender continuously transmits the code word acquired from the data word which follows the control word, until the START OF MESSAGE (SOM) is identified. When Identified, the outgoing codeword stream is replaced with INTERDIGIT (ID) codewords.

The DIBTS sender transmits each message codeword as a block of 20 consecutive repetitions of the codeword. Each message codeword block is allowed by a block of 20 consecutive INTERDIGIT codewords. Following the last message codeword block, ID is sent continuously.

1-30.10.3 DIBTS Receiver. The DIBTS receiver collects the serial DIBTS 16 or 32 kb/s data from the SWITCH DEMUX and detects valid codewords. The DIBTS receiver detects and identifies any of the three supervisory codewords ACK, NACK, and SEIZE ACK, and reports it to the SBC by formatting a receive control word and sending it to the input buffer.

The DIBTS receiver also identifies the SOM codeword and indicates this to the DIBTS sender. It collects the codewords framed by the SOM and END OF MESSAGE (EOM), excluding the 20X redundancy and the ID. If an EOM is not identified within the time spanned by 60 digits, the message assembly is terminated. A receive control word followed by the accumulated message is sent to the input buffer.

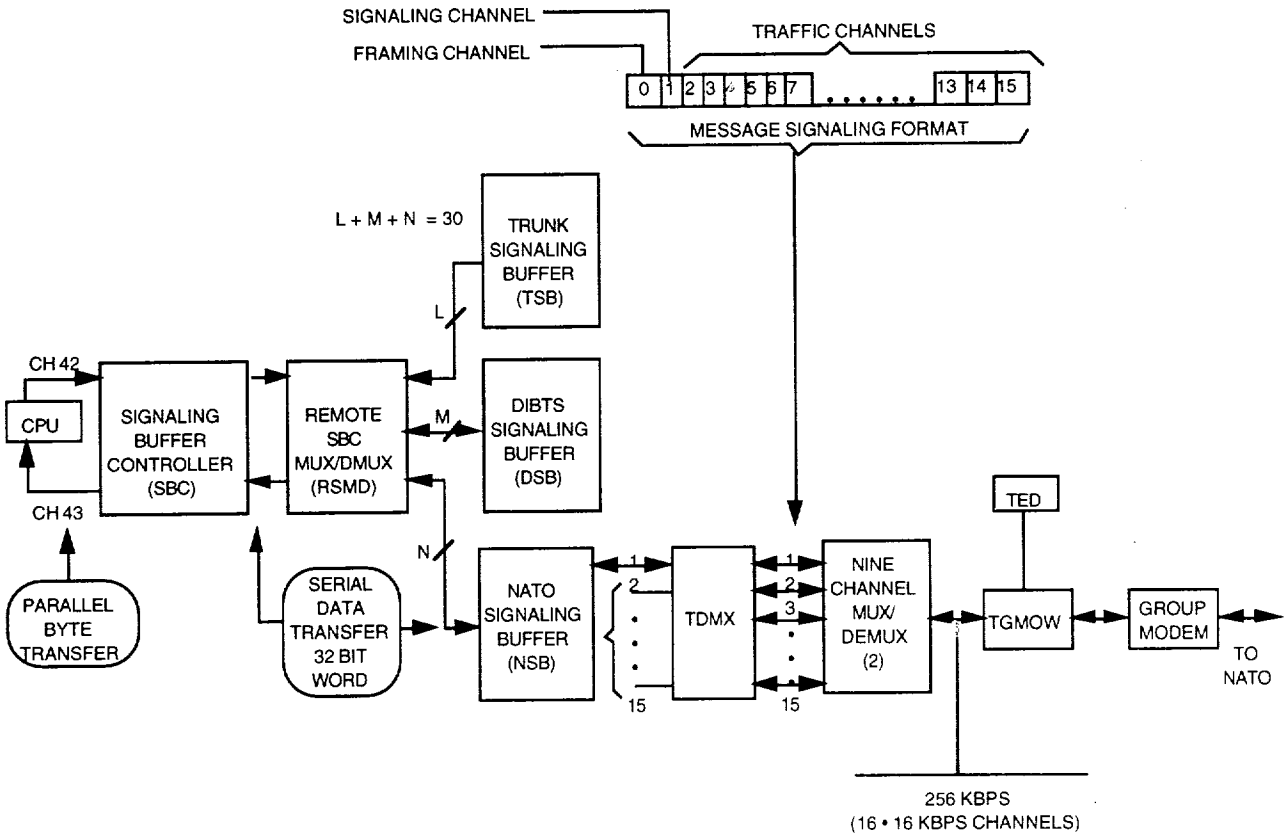
1-30.10.4 Input Buffer. After the input buffer has received the complete message, the SBC INPUT READY is activated. The SBC responds with enable pulses over the SBC INPUT ENABLE line. With each enable pulse one word (32 bits) is emptied from the input buffer. The first pulse resets the SBC input ready line before the next message arrives from the DIBTS receiver.

The DIBTS buffer reset places the DIBTS buffer in the idle state. It clears all the software and hardware buffer registers, resets the CPG and CSS interfaces, transmits the ID code, and places the receiver in the supervisory mode.

1-30.11 Digital NATO. The digital interface to NATO can be implemented over a radio link or a cable link. These DTGs are configured with a compatible cable interface and high voltage assembly. In addition to an NSB, the cable interface also requires a digital NATO group modem (DNGPM) and a digital NATO trunk group module (DNTGM) in place of the GPMDM and TGMOW cards. Digital NATO interswitch trunk signaling uses formatted messages transmitted over a common signaling channel to control the usage of the traffic channels. Digital NATO uses two overhead channels. One channel is used for framing, and a second channel is used for common channel signaling messages (figs. 1-49 and 1-50).

The signaling channel interfaces the NATO transmission group through a digital NATO trunk signaling buffer (NSB) which handles the transmission and reception of trunk signaling messages. The NSB serves as the primary interface between the processor and the transmission medium. It performs forward error detection encoding and decoding, an overall parity check, handshaking with the processor, signaling synchronization, and logic for automatic retransmission on request (ARQ). Each digital NATO trunk group cluster consists of one NATO digital transmission group served by a single NSB. A NATO DTG consists of 16 channels, of which the first is used for framing and the second for common channel signaling. The remaining 14 channels are for traffic. The NSB interfaces the modified TDSG in the same way as a TSB, via the SBC, and is card interchangeable with the existing TSB. The NSB is configured by processor controlled strapping.

The NSB can operate in either the terrestrial or satellite mode. The mode of operation depends on the link interface type and is selected by processor controlled strapping. The terrestrial mode of operation requires the NSB to use a block-by-block acknowledgment scheme and request for retransmission protocol, ensuring the delivery of messages without a message acknowledgment. The request for retransmission protocol refers to a retransmission protocol, ensuring the delivery of messages without a message acknowledgment. The request for retransmission protocol refers to a retransmission scheme when an erred block is received. The request for retransmission contains retransmission block cycle lengths of four or six, depending on the terrestrial link distance. The retransmission block cycle length is referred to as the block-step-back parameters (BSBP). The BSBP is set to four for terrestrial links less than 100 km and six for terrestrial links less than 600 km and greater than or equal to 100 km. The BSBP setting indicates the number of previous information blocks that must be retransmitted during a retransmission request.

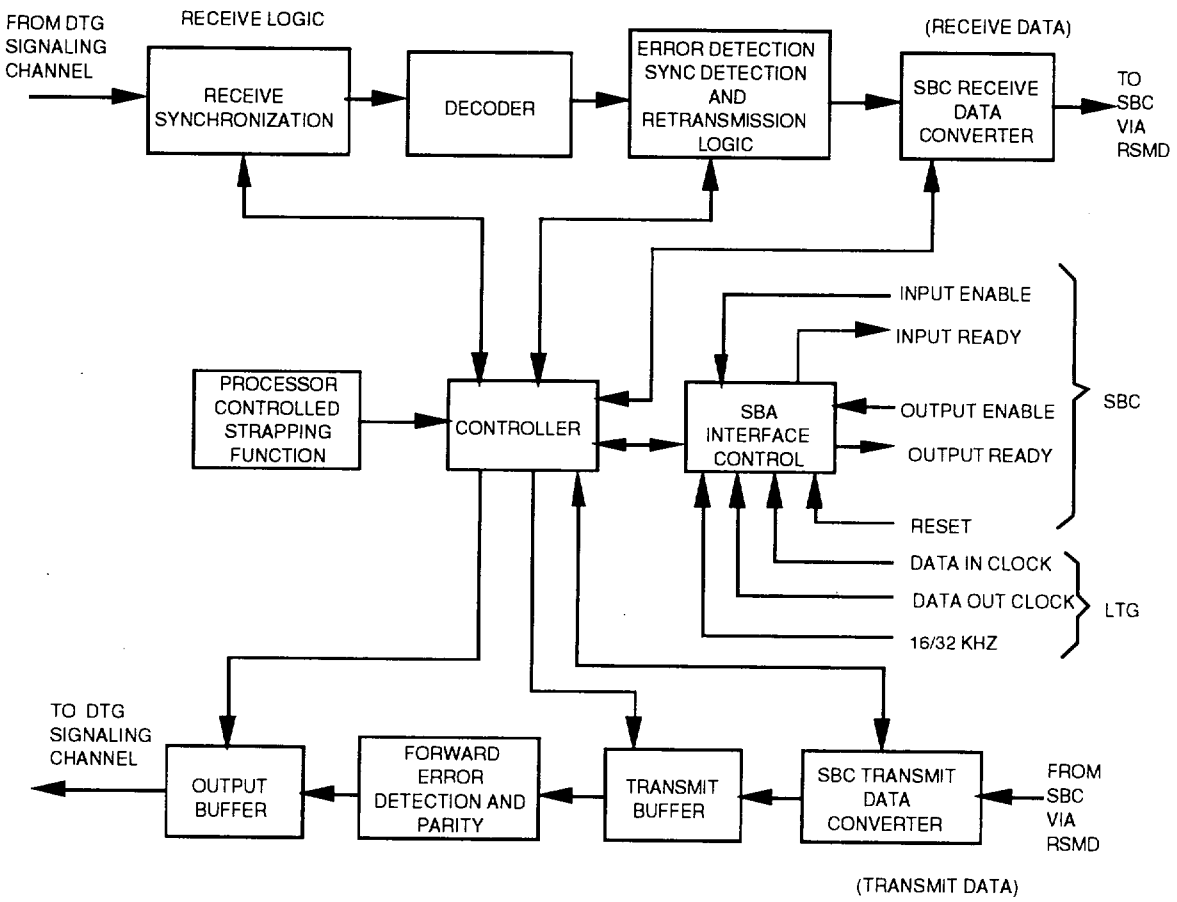


CE2NT780

Figure 1-49. NATO Digital Interface Block Diagram

The satellite mode requires the DNTSB to use a message-by-message acknowledgment scheme controlled by software. In this mode, the DNTSBs BSBP is set to zero, inhibiting the request for retransmission protocol and disregarding the block-by-block acknowledgment scheme unless the NSB enters synchronization. In this mode, the OK/RQ bit is set to one except during synchronization. While in the satellite mode, the NSB retransmits the current message (in 32-bit blocks) over and over until a new message is available. The NSB loads only the received good blocks into a buffer. A complete message can then be assembled in any order over the period in which the current message is transmitted until a new message is received. When a complete message is received, it is transferred to the CPU.

The synchronization procedure consists of the transmission/reception of a 32-bit block containing the 16-bit synchronization code. Synchronization must be achieved in both the receive and transmit direction before signaling information can once again be exchanged. When the receiving NSB is in the synchronization mode, the NSB deletes any partially compiled message and ignores any subsequently received information blocks until it receives a valid block which starts with the SOM field.



CE2NT746

Figure 1-50. NATO Signaling Buffer Block Diagram

The NSB performs in a digital signaling mode. The input/output signaling is at a 16-kb/s data rate over the second overhead channel of the DTG. All subchannels on the signaling channel are completely dedicated to signaling information. All framing is done on the first overhead channel of the 16-channel DTG and is therefore independent of the signaling channel. Error detection is implemented on a per-block basis. Message exchange between the SBC and NSB takes place in groups of 32-bit words.

When a complete message is ready for transmission and the NSB is in transmit synchronization (meaning that the receivers at both ends of the transmission links are in sync), the message is processed in blocks and transmitted. The processing consists of adding the block number, OK/RQ bit, forward error detection, and overall parity. The 32-bit formatted blocks are transmitted continuously with no gaps.

When the interconnection link is via cable interface, modification of the transmission interface is necessary. The DNGPM transmits and receives data between the circuit switch and a NATO digital network circuit switch. The DNGPM provides a balanced line-side interface, with the capability of transmitting/ receiving both traffic and EOW data simultaneously. The transmission/reception of the EOW data is via the DNGPM phantom loop circuit and is possible both in the presence and in the absence of group traffic. The NATO group modem (NGM) provides full duplex transmission of binary signals at a transmission rate of 256 kb/s (16 channels at an individual channel data rate of 16 kb/s).

The transmission mode is diphase, and the medium is via spiral quad cable by means of line drivers. The NGM also provides the phantom loop circuit required for the transmission/reception of the EOW conditioned diphase data.

If a TED is required for a digital NATO gateway, the NATO group modem requires a RED timing source; otherwise, a BLACK timing source is used. The NATO CCS message consists of six basic messages:

- Connection Request
- Routing Attempt Complete
- Called Subscriber Answer
- Release
- Control
- Acknowledgment.

1-30.12 Transmission Group Module/Orderwire (TGMOW). The TGM functionally contains three circuits: the group buffer, the group framing unit, and the group output. These three units, in conjunction with the TED, provide for timing adjustment, encryption and decryption, and frame synchronization of DTG data. The TGMOW circuit card also contains the Engineering Orderwire Signal Processor for transmitting data between the OCU or communications modem and the DTG (fig. 1-51).

The GB receives digital data and a recovered clock from the group modem. This buffer is organized in a FIFO manner such that the data is output by the local switch clock in the same order as input. It is initially set to be 50 percent full and, depending on the difference of the two clock rates, gradually empties or fills. The buffer is adaptive in that the buffer size is varied from 64 to 512 bits to reduce delay at low multiplexed frequencies while increasing the time before overflow occurs at high multiplexed frequencies. The state of the buffer is continuously monitored for a full or empty condition.

This status is available to the processor (via the SCG) as a FIFO full/empty status bit in the TGM status report. When two adjacent switches are bit synchronized to their own atomic frequency references, the buffers should not overflow more frequently than once in 24 hours.

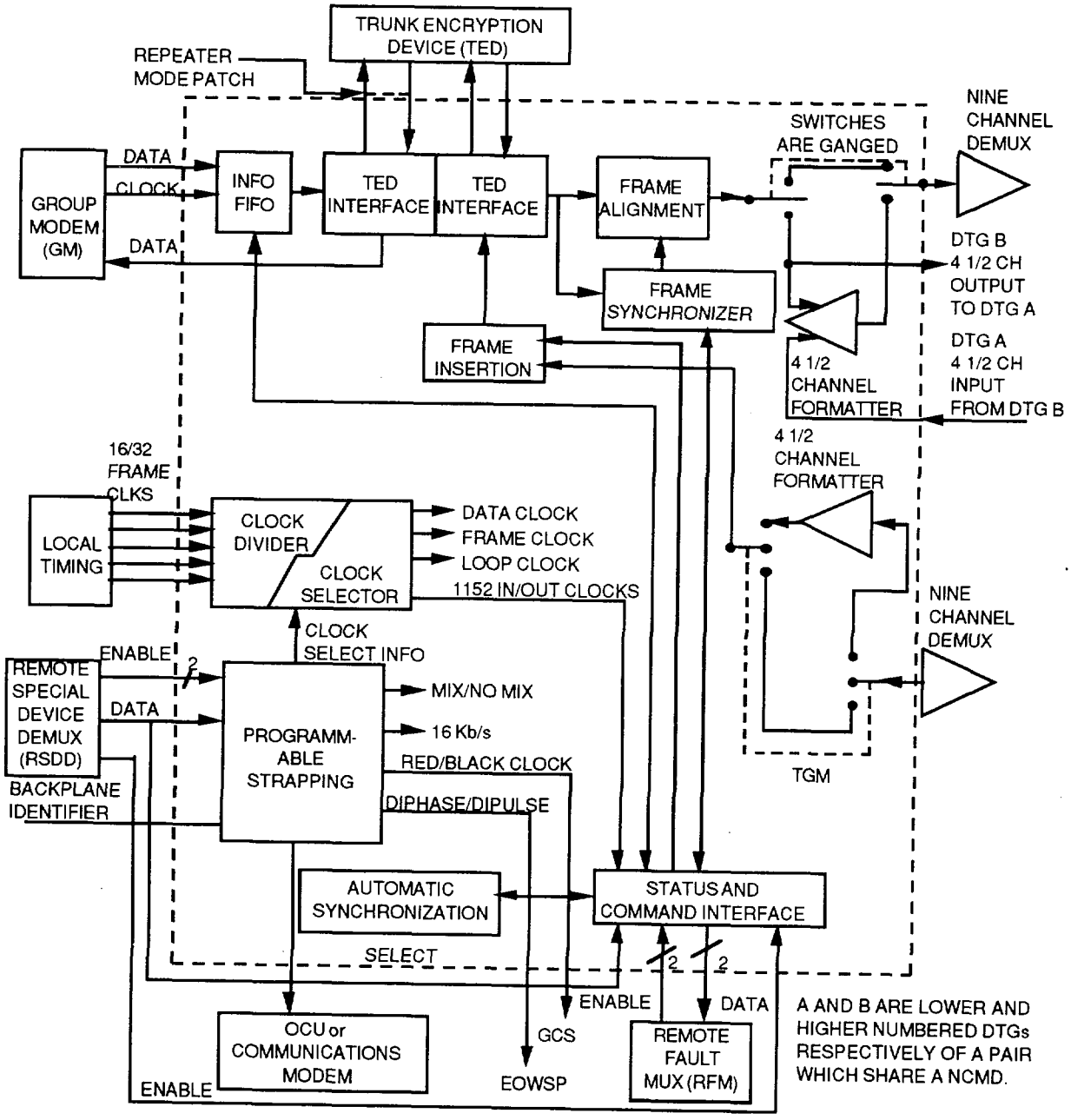
The frame synchronization and monitoring (FSM) circuits monitor the bit stream for a 1010 pattern in the master frame position and traffic on the data channels. During a resynchronization, a frame request pattern of all ONEs in the framing channel and all data channels set to ZERO is transmitted. The FSM circuits, upon receiving a frame request, inhibit the data channels in the ZERO state and continue to send 1010 in the framing channel. The search mode is used to detect these framing patterns.

In search mode the FSM performs a multistage frame acquisition process. During the first level of acquisition. the unit searches the data stream for the leading one of a prospective frame pattern, and then examines every other suspected frame bit position (skipping the ZEROs of the ONE-ZERO pattern). Successful identification of two correct bits of those examined allows the FSM to proceed to the second acquisition level. Once again, every other bit position is checked for the presence of a ONE. More than one error in the next three bits examined sends the unit back to level one. Identification of two out of three bits as correct allows progression to level three. At this point, two detectors are used to examine each of the next 32-bit positions for at least 30 correct bits of either the ONE-ZERO or all ONEs framing pattern. If more than two errors are found by both detectors, the unit returns to level one. Otherwise the unit exits the search mode. At the third level, a check is made of the data channels to assure that they are ZERO. A separate detector is used to examine all data channels for at least 145 ZEROES in 200 bits. Failure to meet this criterion sends the GFU back to level one.

The synchronizing buffer aligns the framing signal recovered from the DTG to a switch generated framing signal. Thus, all framing signals as seen by the TDMX occur at the same time reference.

The output control of the TGM effects the data inhibit and frame pattern changes. It replaces the 1100 subchannel framing pattern inserted in the master frame position (channel 1) by the TSB with the appropriate major channel framing pattern.

The level converter converts the bipolar TED interface signals to the TTL level signals required by the group modem. The interface and timing control circuits provide for the command and status interface with the SCG and the processor, and manual synchronizing inputs that allow manual activation of the resynchronizing command lines.



CE2NT747

Figure 1-51. Transmission Group Module/Orderwire Block Diagram

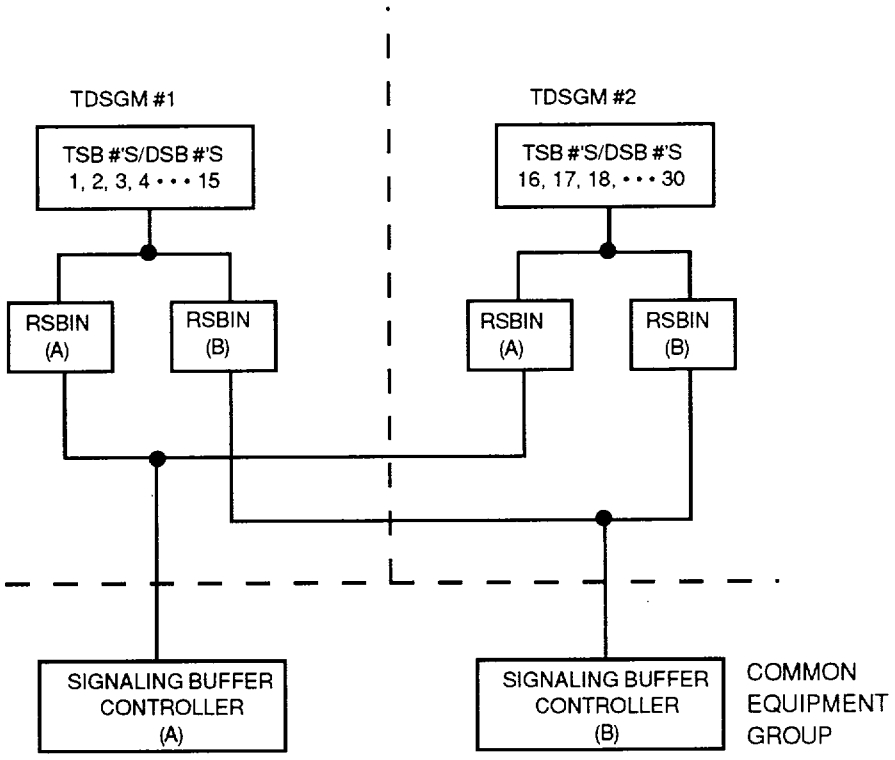
Synchronization of the incoming data to the system framing reference is accomplished by the frame synchronizer. The group output section includes circuitry for formatting the DTG input and output for 4 1/2 channel DTGs.

A five-bit input and a five-bit output address is employed to select the gate data input and output signaling between any trunk signaling buffer, NATO signaling buffer or DIBTS buffer, and the signaling buffer controller. Line drivers and receivers are employed for sending and receiving the signaling buffer controller data, address, and reset signals.

A reset capability exists whereby the signaling buffer controller may at any time address an individual trunk signaling or DIBTS buffer, and activate that unit's master reset. This signal is gated through the RSBIN. In addition, a system master reset capability exists whereby the signaling buffer controller may at any time activate the master reset lines of all TSBs and DSBs.

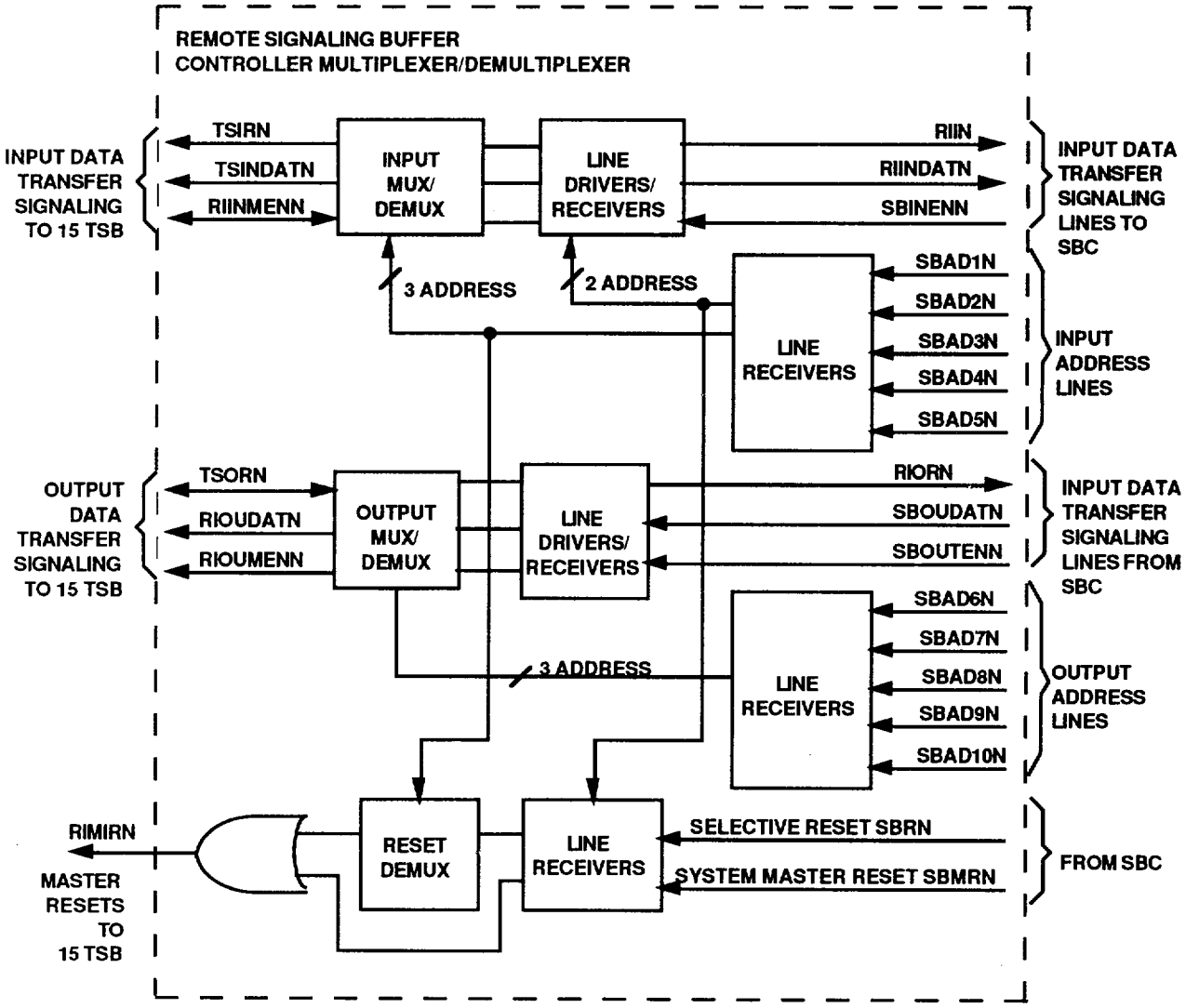
The selective and system master resets are two different lines coming to the RSBIN from the signaling buffer controller. They are logically gated together within the RSBIN and only one master reset line is connected from the RSBIN to each TSB, NSB, and DSB.

1-30.13 Remote Signaling Buffer Controller Multiplexer/Demultiplexer (RSBIN). The RSBIN is used to transfer input and output data between the TSB, NSB, or the DSB and the SBC. The RSBIN provides the multiplexing and demultiplexing necessary to interface 15 trunk signaling buffers and/or DIBTS buffers. Two RSBIN cards are provided with each TDSG to interface the 15 TSB/NSB/ DSBs to the redundant SBCs (figs. 1-52 and 1-53).



CE2NT748

Figure 1-52. Signaling Buffer Controller Multiplexer/Demultiplexer Usage Block Diagram



CE2NT749

Figure 1-53. Remote Signaling Buffer Controller Multiplexer/Demultiplexer Block Diagram

The input multiplexer/demultiplexer provides the interface for input data transfer signaling from the trunk signaling buffer or the DIBTS buffer to the signaling buffer controller. The output multiplexer/demultiplexer provides the interface for output data transfer signaling to the trunk signaling buffer and DIBTS buffer units from the signaling buffer controller.

A five-bit input and a five-bit output address is employed to select the gate data input and output signaling between any trunk signaling buffer, NATO signaling buffer or DIBTS buffer, and the signaling buffer controller. Line drivers and receivers are employed for sending and receiving the signaling buffer controller data, address, and reset signals.

A reset capability exists whereby the signaling buffer controller may at any time address an individual trunk signaling or DIBTS buffer and activate that unit's master reset. This signal is gated through the RSBIN. In addition, a system master reset capability exists whereby the signaling buffer controller may at any time activate the master reset lines of all TSBs and DSBs.

The selective and system master resets are two different lines coming to the RSBIN from the signaling buffer controller. They are logically gated together within the RSBIN and only one master reset line is connected from the RSBIN to each TSB, NSB, and DSB.

1-30.14 Essential User Bypass Selector. The EUB selector provides an automated capability to bypass preselected digital subscribers or SEN/RAU trunk groups to a distant circuit switch (fig. 1-54). It does this in case both processors of a circuit switch fail. The EUB selector provides the capability to store 124 from/to connection addresses, one test address (to connect a digital signal generator tone to a test point) and 15 reset (all location) commands (one per TDMM).

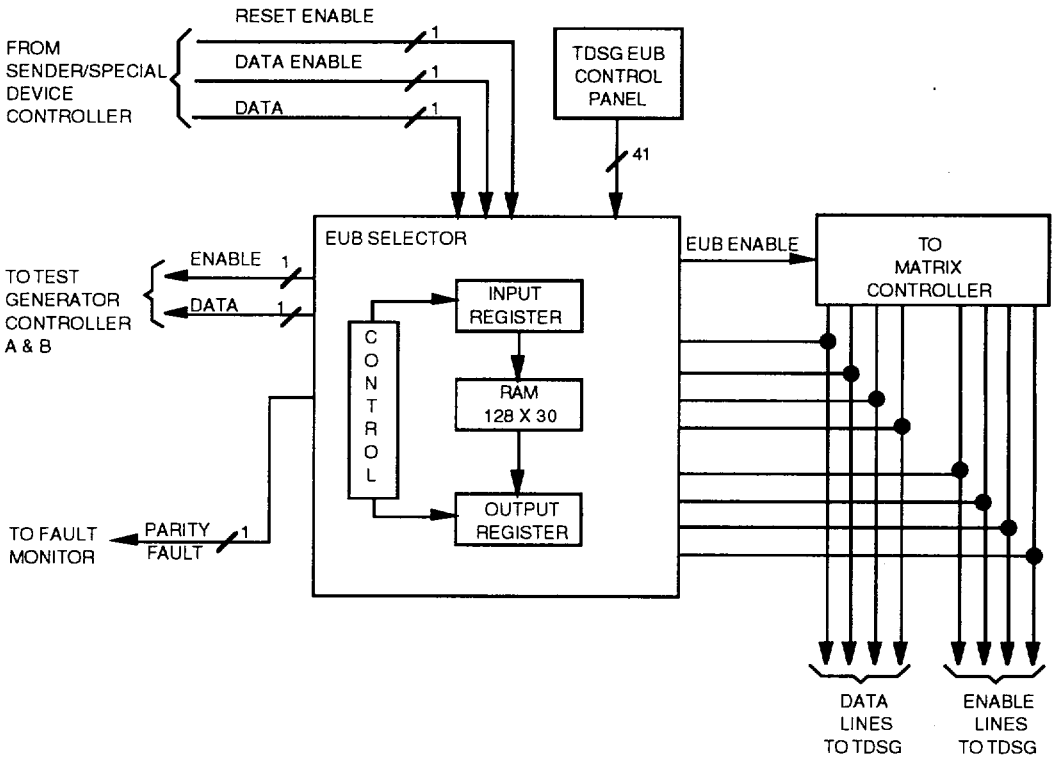
Upon activation of the EUB function (from the EUB control position of the patch and control panel), the EUB selector transmits, in sequence, the 15 stored reset (all location) commands and the 124 stored connection commands. Upon activation of the load switch, the selected from/to address is accepted by the EUB selector, formatted into a full connect command and delivered to the TDMM.

When in the EUB mode, the EUB selector appears to the TDSG as though it were the SCG matrix controller. When not in the EUB mode, the EUB selector is disconnected. Built-in test equipment is provided as part of the EUB selector. It permits testing (through the SCG test generator controller) and enables it to perform a continuous parity check of its stored addresses.

1-30.15 Remote Signaling Buffer. The RSB/DA, upon processor controlled strapping, performs the function of either two RSB circuits or one RSB circuit and one DA circuit. Each RSB circuit provides an interface between the remote signaling buffer interface (RSBIN), which is an extension of the SBC, and the routing subsystem (RSS) signaling channel which occupies one 16 kb/s channel of a DTG. Each RSB has a dedicated full-duplex port on the TDMX such that it can be connected to the RSS signaling channel of any DTG. The DA circuit has an interface either between the RSBIN and a System Control Center (SCC)/Interswitch trunk or between an SCC/Interswitch trunk and an asynchronous, serial, RS-422, interface to the Node Management Facility (NMF). Like the RSB, the DA circuit has a dedicated full duplex TDMX port such that it can be connected to any SCC trunk or any interswitch trunk. Figure 1-55 shows a typical application of the RSB/DA in a flood search routing network. A functional block diagram is provided in figure 1-56. The interfaces of the RSB/DA are defined in table 1-8.

All signals, except the NMF input and output, are TTL levels. TTL levels assign 0.0 to 0.8 V to the logic one state, and 2.0 to 5.5 V to the logic zero state. The NMF interface is an asynchronous, serial, RS-422 interface used to allow communication between the local NMF and either a remote NMF or an SCC. The baud rate for the interface is either 1200, 2400, 4800, or 9600 baud dependent upon Special Device Strapping. The character format on this interface is 1 start bit (logic 0), 7 data bits, 1 odd parity bit, and 1 stop bit (logic 1).

The RSS Signaling Channel/TDMX interface is a standard TTL interface to the TDMX at 16 kb/s. The bit coding for this channel is Non-Return to Zero (NRZ). Bytes are transmitted and received least significant bit first. The two error control bytes contain a Cyclic Redundancy Check (CRC). In the case of consecutive messages, the end flag of the first message shall be the start flag of the next message.



CE2NT750

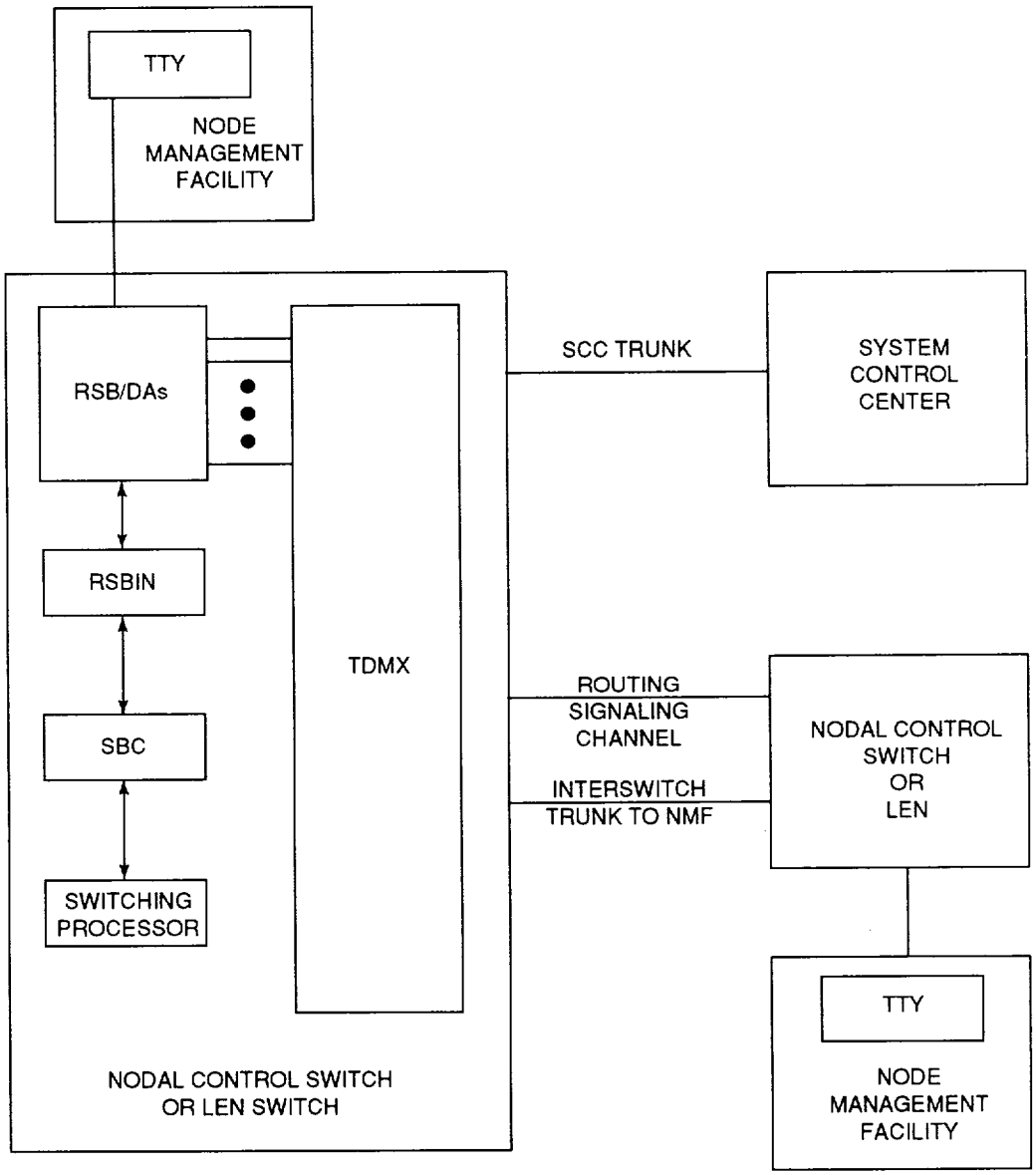
Figure 1-54. EUB Selector Block Diagram

Table 1-8. Interface Definition

SIGNAL	SOURCE	DESTINATION	DESCRIPTION
RSB Input	TDMX	RSB/DA	Serial interface to receive flood search signaling from a connected switch
RSB Output	RSB/DA	TDMX	Serial interface to transmit flood search signaling to a connected switch
Data Adapter Input	TDMX	RSB/DA	Serial interface to receive operational and technical messages from an SCC or NMF
Data Adapter Output	RSB/DA	TDMX	Serial interface to transmit operational messages to an SCC or NMF
NMF Input	NMF	RSB/DA	RS-422 serial interface to receive messages from NMF
NMF Output	RSB/DA	NMF	RS-422 serial interface to transmit messages to NMF
Card Presence	RSB/DA	Fault controller	Pull to 0V
Power	Power processor	RSB/DA	DC power

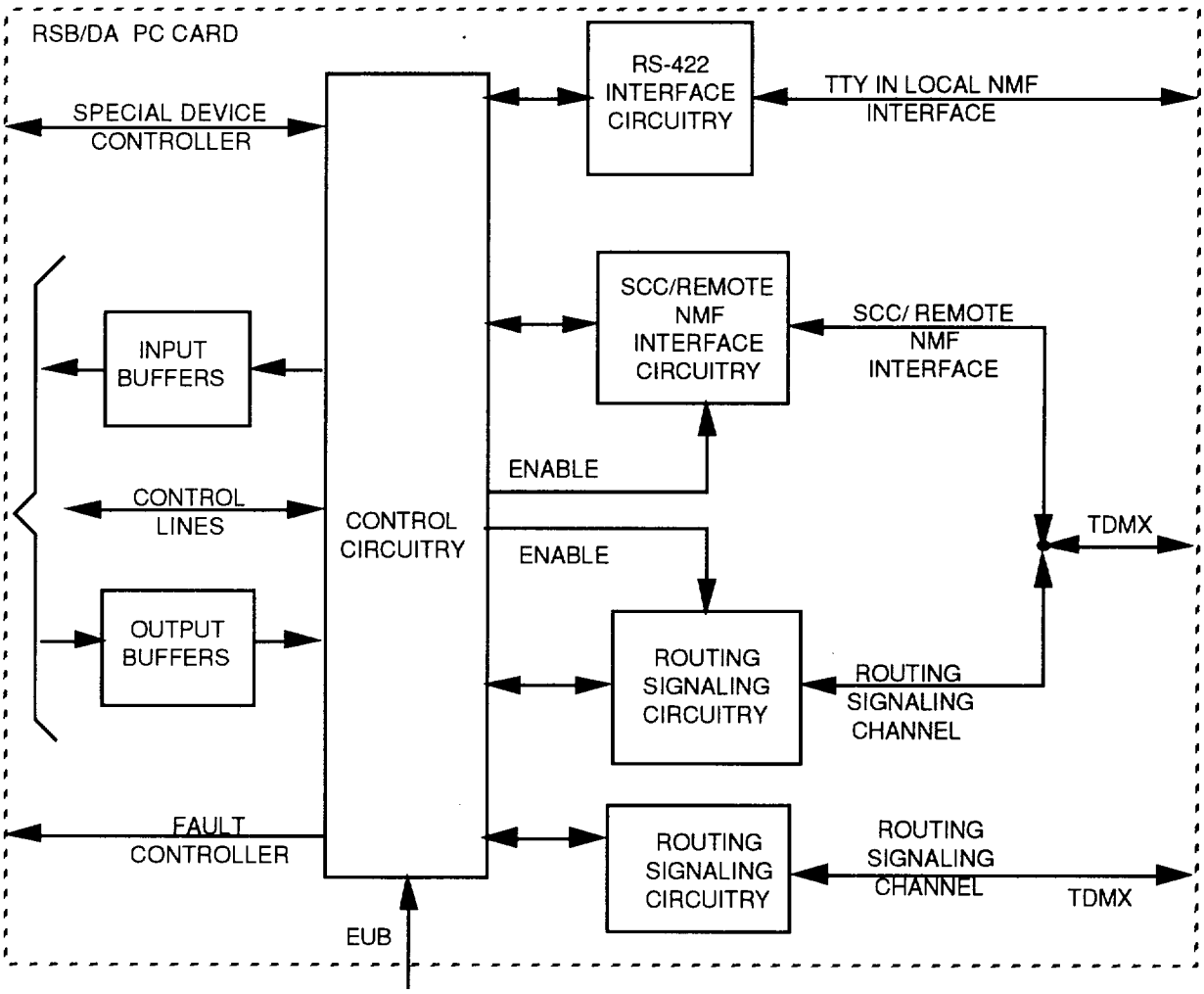
Table 1-8. Interface Definition - Continued

SIGNAL	SOURCE	DESTINATION	DESCRIPTION
Clocks	Local timing generator	RSB/DA	TTL level clocks
EUB Mode Indicator	EUB selector or matrix controller or LTBF	RSB/DA	TTL level signal which indicates if the switch is in EUB mode or not



CE2NT751

Figure 1-55. RSB/DA in a Flood Search Routing Network Block Diagram



CE2NT752

Figure 1-56. RSB/DA Functional Block Diagram

If the RSB/DA circuit is strapped for RSB operation, then signaling messages from the SBC interface are transmitted to the RSS signaling channel as follows. If a signaling message is received from the SBC, the RSB/DA strips the Transmit Control Word from the Message Data Field bytes and adds a start flag, message control field indicating signaling message, error control bytes, and an end flag to the Message Data Field bytes. In order to avoid flag imitation in the frame data field and error control bytes, an additional zero bit is transmitted after a sequence of five consecutive one bits is encountered. The RSB/DA then transmits the message to the RSS signaling channel. When no signaling messages are being transmitted on the RSS signaling channel, the RSB/DA transmits continuity messages. Signaling messages received from the RSS signaling channel are sent to the SBC interface as follows: Continuity messages received from the RSS signaling channel are not to be sent to the SBC interface. If a signaling message or a continuity message is received from the RSS signaling channel, the RSB/DA scans the message for the start flag. The end flag should be within 16 bytes following the start flag.

If a sequence of five consecutive one bits is encountered in the frame data field or error control bytes, the next bit is deleted from the message. The RSB/DA performs error checking by generating a CRC based on the bytes of the Frame Data Field of the received message. If the CRC that is generated is equal to the CRC bytes which were transmitted in the message, then the RSB/DA strips the start flag, the error checking bytes, and the end flag and sends the signaling message to the SBC. If an end flag is not detected within 16 bytes following the start flag, or if error checking indicates a detected error, the RSB/DA considers the message to be invalid and discards the message.

The SCC/interswitch trunk/TDMX interface is a standard TTL interface to the TDMX at 16 kb/s. A data call is set up prior to the transmission of messages over this interface. There are three types of frames that are transmitted and received over this interface: data frames (DFs), start frames (SFs), and ACK frames.

The message that is sent to the SCC/interswitch trunk interface is composed of a SF, followed by a number of DFs. The SF shall contain a frame number of zero, the number of frames (NF) field shall contain a value representing the number of DFs contained in the message, and the number of data bytes (NB) field will contain a value representing the number of data bytes of the DFs contained in the message. The frame number field of the DFs shall contain a value representing the frame number.

Messages from the SCC/interswitch trunk interface are transmitted either to the SBC or the NM F interface. The RSB/DA determines if a message should be routed to the SBC or the NMF based upon a data type message.

Upon receipt of a valid start or data frame, the RSB/DA strips the start flag, the error checking bytes, and the end flag, stores the remainder of the start frame and returns a start ACK or data ACK to the SCC/interswitch trunk.

The RSB/DA communicates with the SBC using 32-bit words. Bit 32 of each word is transmitted and received first.

If the RSB/DA circuit is strapped for DA operation, then messages from the SBC or the local NMF interface for subsequent transmission to the SCC/Interswitch trunk consist of an Answer message in response to a Technical message from the SCC. If a frame is received from the SBC, the RSB/DA takes the Message Data Field bytes and adds a start flag, error control bytes, and an end flag. The result is either an SF or a DF.

If a message is received from the NMF interface, the RSB/DA divides the message consisting of the Front of Transmit Envelope (FTE) field, the End of Line (EOL) field, the data field, and part of the End of Transmit Envelope (ETE) field into data blocks, each containing four bytes. Padding bytes of ZEROs are used whenever necessary in the last data block to complete the block. To each data block, the RSB/DA adds a start flag, error control bytes, and an end flag. The result is a data frame.

1-30.16 Nine Channel MUX/DEMUX (NCMD). The NCMD provides for the time combination of individual 16 kb/s digital bit streams from the switch mux/demux into one bit stream for input/output to the DTG equipment and loop mux/demux. The bit rate of the combined channel bit stream is compatible with the DTG rate by programming the appropriate number of NCMD units into the proper serial sequence and bit rate. The NCMD is compatible with strategic (modularity of nine) or tactical (modularity of eight) DTG rates. The demux register uses a serial-toparallel shift register to select the proper 9/8 bits from the input bit stream. The input bit stream is common to all NCMDs used to demux a single DTG. The buffer outputs the data on all channels synchronously with the framing signal (fig. 1-57).

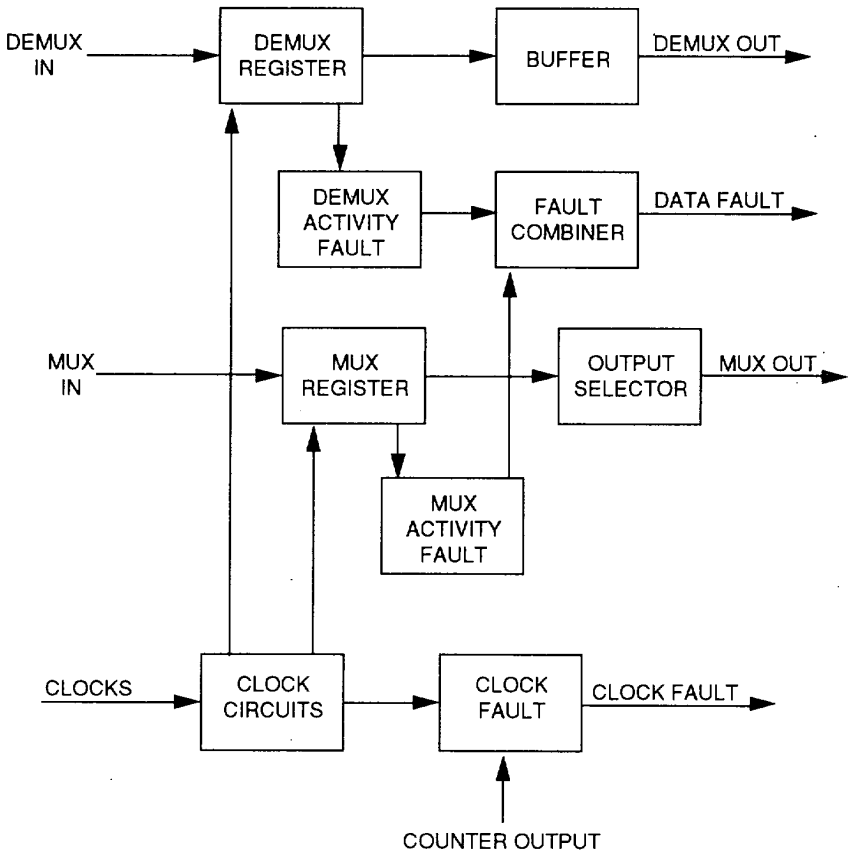


Figure 1-57. Nine Channel Mux/Demux Block Diagram

The mux register is a 9/8 bit parallel-to-serial shift register. Mux registers in all NCMDs interface to a single DTG, and are interconnected to form a large parallel-to-serial shift register. The data is clocked in by the framing signal and clocked out by the transmission group rate clock.

The output selector determines whether the mux out signal is delivered to the next NCMD in the chain or output to the DTG equipment. Clock circuits select the transmission group rate clock and provide timing for the mux and demux registers.

Fault indications consist of a DATA FAULT and a CLOCK FAULT. The DATA FAULT monitors the mux and demux data streams for data transitions. The CLOCK FAULT compares its counter with its neighbor's counter and monitors for clock transitions.

Several NCMD multiplexing sections are connected in series, as shown in figure 1-58, to assemble long streams of data to accommodate the DTG modularities. The dashed line in figure 1-58 shows the connections for all three NCMDs used for TGM number 1. Each of the NCMD multiplexing sections contains logic to select the destination of its serial output. The output may be directed to the next NCMD or to one of eight DTGs or LMDs. Only one output can be selected at a time and, when one is selected, the other seven drivers are turned off since they use tri-state outputs. The NCMDs consist of two separate NCMD chains. Each has 36 NCMDs divided into two groups of 18, each of which interfaces to a different set of transmission groups. The selection is performed by autostrapping via the special devices controller. A bit identifies the first card in a chain of NCMD operations on each DTG.

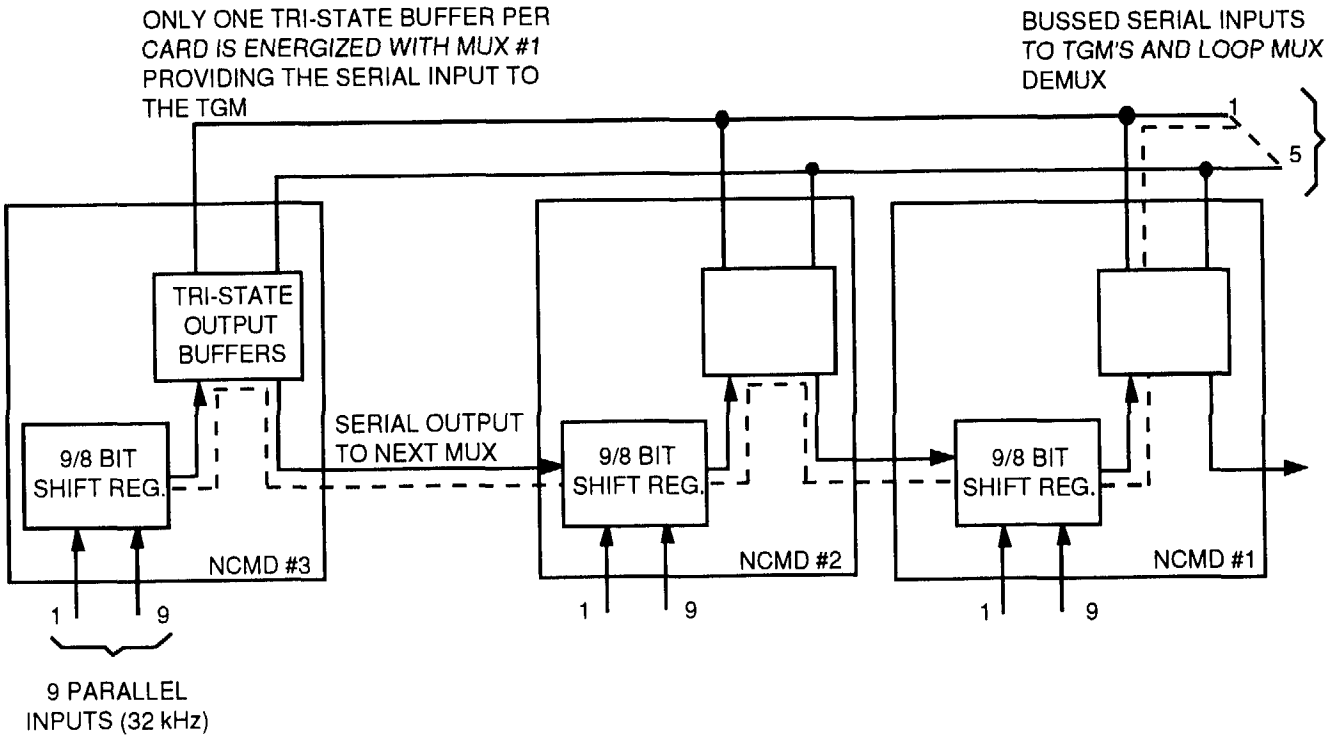


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Figure 1-58. Interconnection of Multiplexer Stages

The interconnection of demultiplexers to handle lengthy streams of data bits is shown in figure 1-59. This operation differs from the interconnection of the multiplexer sections in that the serial data stream in demux number 1 does not pass through demux number 2. Each demux has its own serial input from the selected source. When the framing pulse occurs, demux number 1 shifts in the serial data while its counter maintains a count of the number of bits being clocked into the 9/8-bit shift register. When 9/8 bits are clocked in, they are shifted into a holding register and the next NCMD in the chain is notified by setting the NCMD number 1 FULL indicator. Demux number 2 performs the same procedure that demux number 1 finished, initiated by the FULL indicator rather than the framing pulse. All demuxes in the chain perform this function in turn.

1-30.17 Digital Signal Generator. The DSG generates all codewords and digitized tones required by the TDSG and TDSG subscribers. The DSG provides the 20 even-parity eight-bit permutable codewords used for signaling and supervision by digital loops. The DSG also provides digitized tones and recorded announcements for both digital and analog loops terminating on the TDSG. The DSG output bit stream consists of a 64-channel multiplexed data stream which interfaces the TDMX. Each codeword or digitized tone is switched by the TDMX to all desired locations (fig. 1-60).

The DSG contains a codeword storage area, digitized tone storage area, clocking circuitry, FSK-on/off control circuitry and a 64-bit shift register. Each analog tone is stored as a digital bit pattern in a read-only memory (ROM) in the DSG. The original analog waveform is reconstructed when the stored digital stream is passed through a CVSD unit. The codewords needed for supervision are likewise stored in a ROM in the DSG. In addition, four recorded announcements are sent to the 64-bit shift register by the intercept recorders.

Clocking circuitry provides timing in the DSG for the memory addressing and multiplexing operation. This circuitry increments the address counters at a 16 kb/s rate to provide proper loading of the 64-bit shift register. The output data stream is shifted out to the TDMX at a 1.024 Mb/s rate.

The FSK on/off control circuitry provides the timing for the dual tone and on/off tone signals required for supervision and editing.

The tones, codewords, and recorded announcements are multiplexed into a 64-channel, 1.024 Mb/s output data stream by the 64-bit shift register. The output data stream is sent to all TDMMs.

1-30.18 Digital Receiver (DR). The DR detects address signals generated by the calling subscriber terminal during call initiation. When the processor determines that a caller is waiting for dialing service, it directs that a DR be connected to the plain text inlet of the calling terminal and sends dial tone to the subscriber. For unencrypted service, the DR is connected directly to the loop, whereas for encrypted service, the DR is connected to the plain text side of the loop crypto receiver (fig. 1-61).

The operation of the DR is illustrated in figure 1-62. In the standby (available) condition, the DR is in state A, connected to an all ONEs signal. When a subscriber wishes to place a call by going OFF-HOOK, the subset transmits the SEIZE signal. Upon detection of SEIZE, the processor assigns an available DR to the calling loop and sends DIAL signal to the subset. Advancement to state B (fig. 1-62) takes place only if the INTERDIGIT (ID) signal is detected by the interdigit decoder. This event occurs when the subset responds with the repeated ID codeword (alternating 1s and Os) after sensing the DIAL signal. For an encrypted call, the calling loop crypto equipment must successfully synchronize before INTERDIGIT appears at the DR input. The subscriber dials the called party address by sequentially operating the 16-button keyset, depressing one button at a time. Activation of two buttons simultaneously will cause a dialing error. A digit codeword is generated by the subset when the subscriber depresses each button. INTERDIGIT is generated between digit bursts.

When the DR successfully recognizes any eight-bit permutable codeword while in state B, or INTERDIGIT while in state A, the detected codeword is sent to the processor. The input register stores nine bits such that the first and ninth can be compared. The counter looks for 32 consecutive successful comparisons from the input register; thus, successful detection of four consecutive permutable codewords is required to produce a message to the processor. A properly detected codeword is stored in the output register for subsequent transfer to the processor.

At the end of dialing, the DR is removed from the calling loop and connected to all ONEs to await assignment to another call. Upon detection of all ONEs by the ONEs decoder, the output register is inhibited. The all ONEs signal is not reported to the processor.

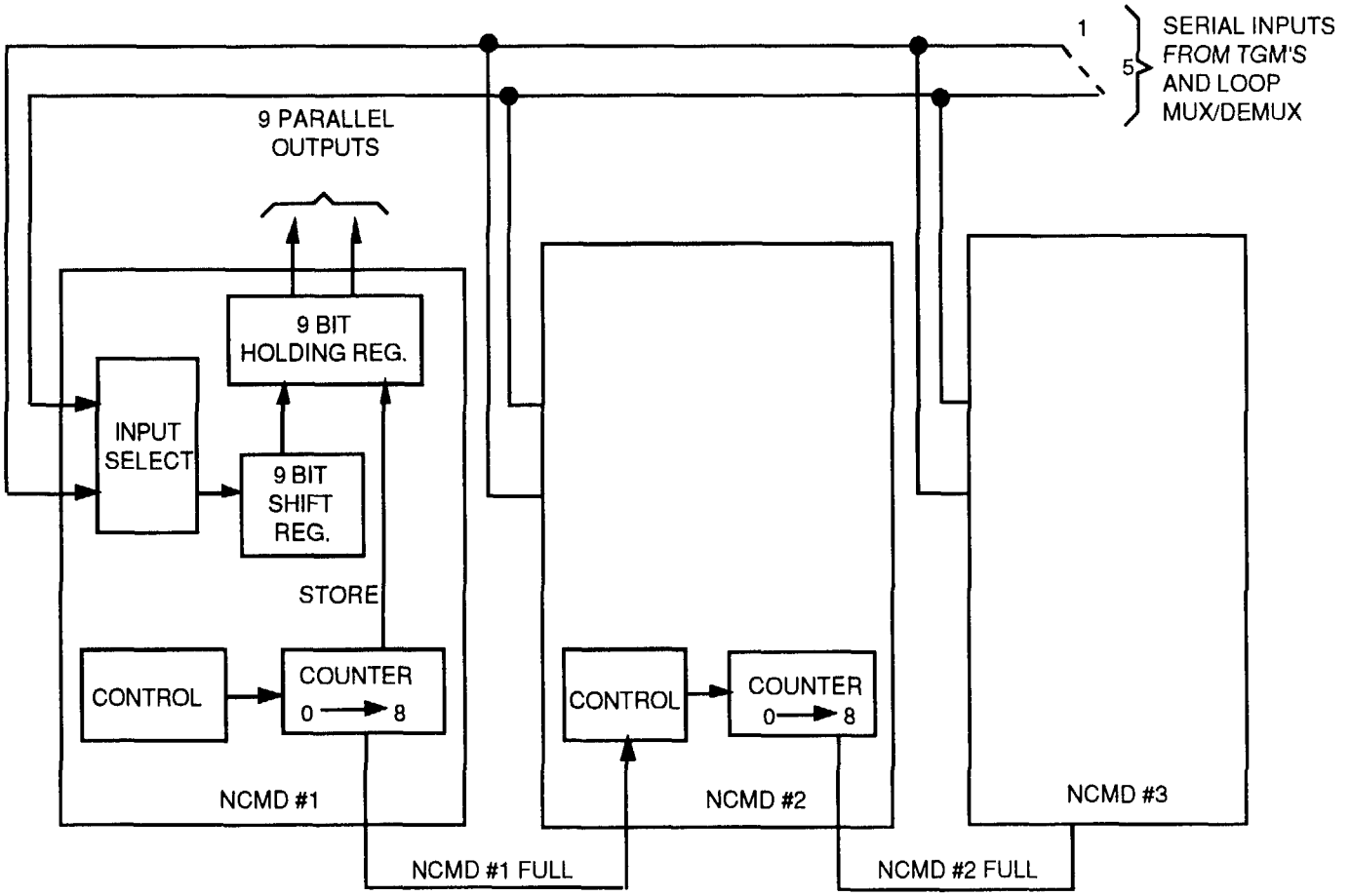

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Figure 1-59. Interconnection of Demultiplexer Stages

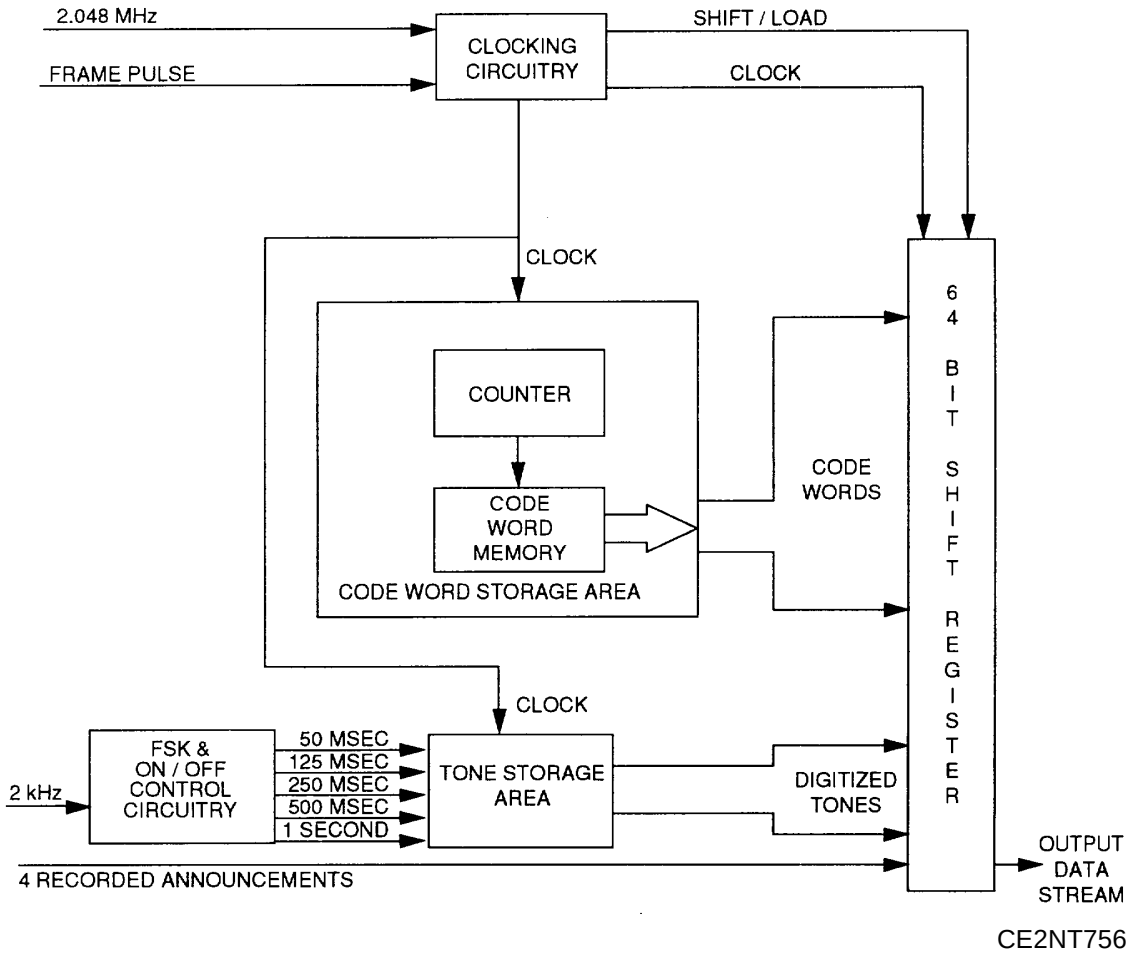


Figure 1-60. Digital Signal Generator Block Diagram

1-30.19 Loop Multiplexer/Demultiplexer. The loop multiplexer combines up to 64 32/16-kb/s loop subscribers from the DLTU modulation unit or diphase loop modem-A into a 64-channel multiplexed data stream which is sent to the group multiplexer. Conversely, the loop demultiplexer accepts the data stream output of the group demultiplexer and splits it into individual 32/16-kb/s digital data streams. The loop multiplexer/demultiplexer uses the same equipment as the common equipment mux/demux.

1-30.20 Common Equipment Multiplexer/Demultiplexer. The common equipment multiplexer combines up to 64 32/16-kb/s channels into a 64-channel multiplexed data stream which is sent to the TDMM. The common equipment multiplexer interfaces the RSB/DSB buffers, the CVSDs which interface the CBUs, and the auxiliary sender/receiver. The common equipment multiplexer also interfaces the LKGs, digital receivers, and the DLPMAs for the CSP digital interface.

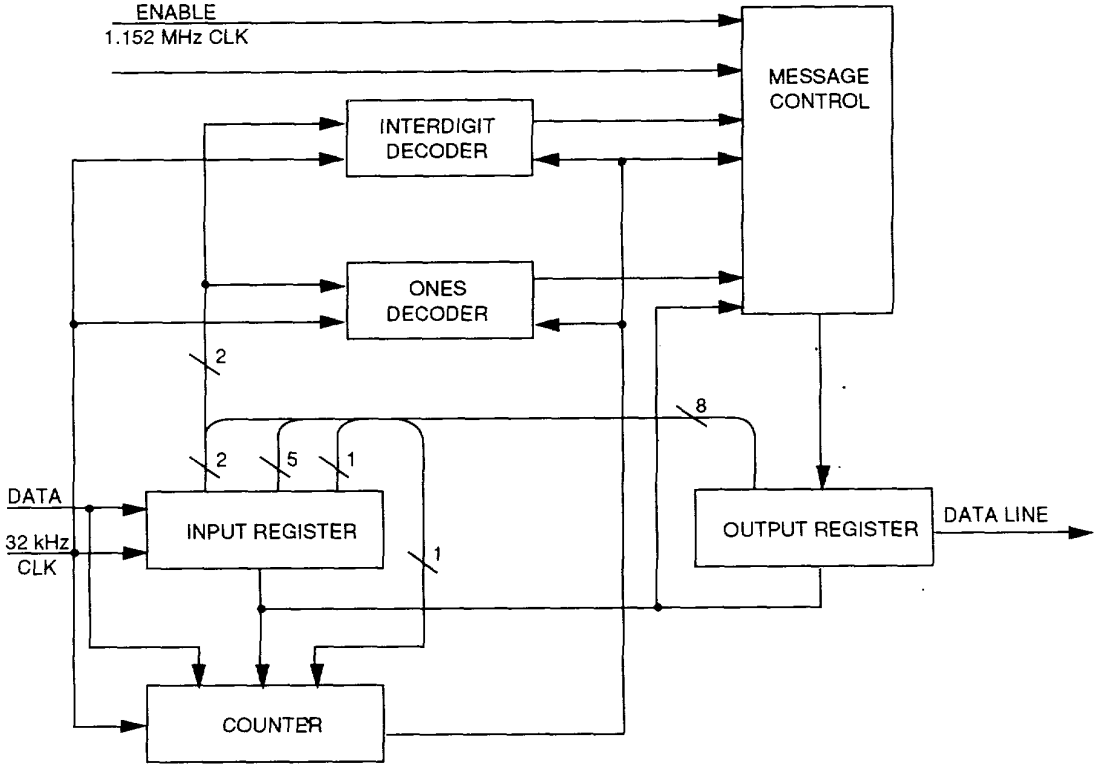
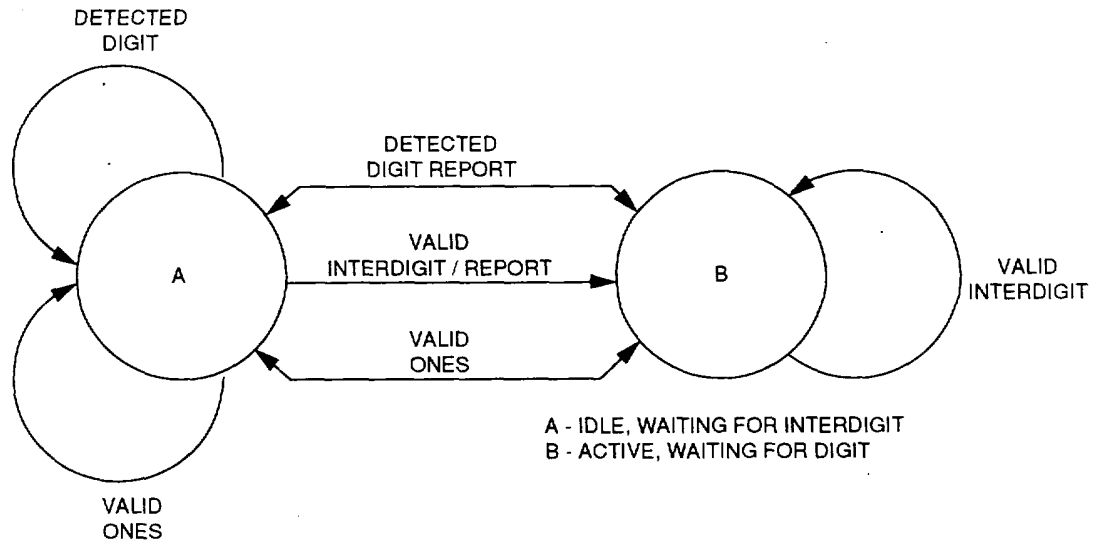


Figure 1-61. Digital Receiver Block Diagram



DIGIT = ANY 4 IDENTICAL AND CONSECUTIVE 8 - BIT WORDS OTHER THAN INTERDIGIT (10101010 OR 01010101 OR ONES (11111111)

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Figure 1-62. Digital Receiver Operation

1-31 PACKET SWITCH HOST/TRUNK INTERFACE (PSHTI).

The PSHTI card is used to interface packet switch ports to the matrix, through which they are connected to trunk or host lines. The PSHTI converts the RS-423A interface from the PS to a TTL interface to the matrix. (fig. 1-63).

Each card interfaces up to three PS ports to the TDSG. If channel 1 is a trunk the 64 kb/s channel is demultiplexed to four adjacent TDMX terminations, which are routed as a group, and channels 2 and 3 are disabled. If channel 1 is a host (or 16 kb/s trunk) the other two channels may also be hosts which are routed to individual terminations.

The PSHTI card hardware configuration is set by manual strapping on the card and is displayed on lights at the edge of the card. The hardware setting must agree with the PS software configuration. The PSHTI card is transparent to the protocols sent over the lines. The trunk strapping is used for connection to 64 kb/s ports and the host strapping is used for 16 kb/s ports, including SEN trunk ports.

When routing is over poor quality transmission links Forward Error Correction (FEC) can be manually switched into the link. The FEC is compatible with FEC at another PSHTI card or TMIF at the other end of the link.

1-32 TRANSCEIVERS (XCVRs).

The CC uses five transceivers. Each XCVR converts the twisted-pair Ethernet interface present on the PSs and HWS to a thin LAN interface compliant with IEEE 802.3. Two local area networks (LANs), each capable of handling up to 30 hosts, connect to the MSE packet network at the CC signal entry panel (SEP). Each LAN connects to a packet switch through a XCVR. The remaining XCVR is used to connect the workstation, which is a LAN host, to one of the LANs and thus interface the HWS to the packet network for electronic mail service.

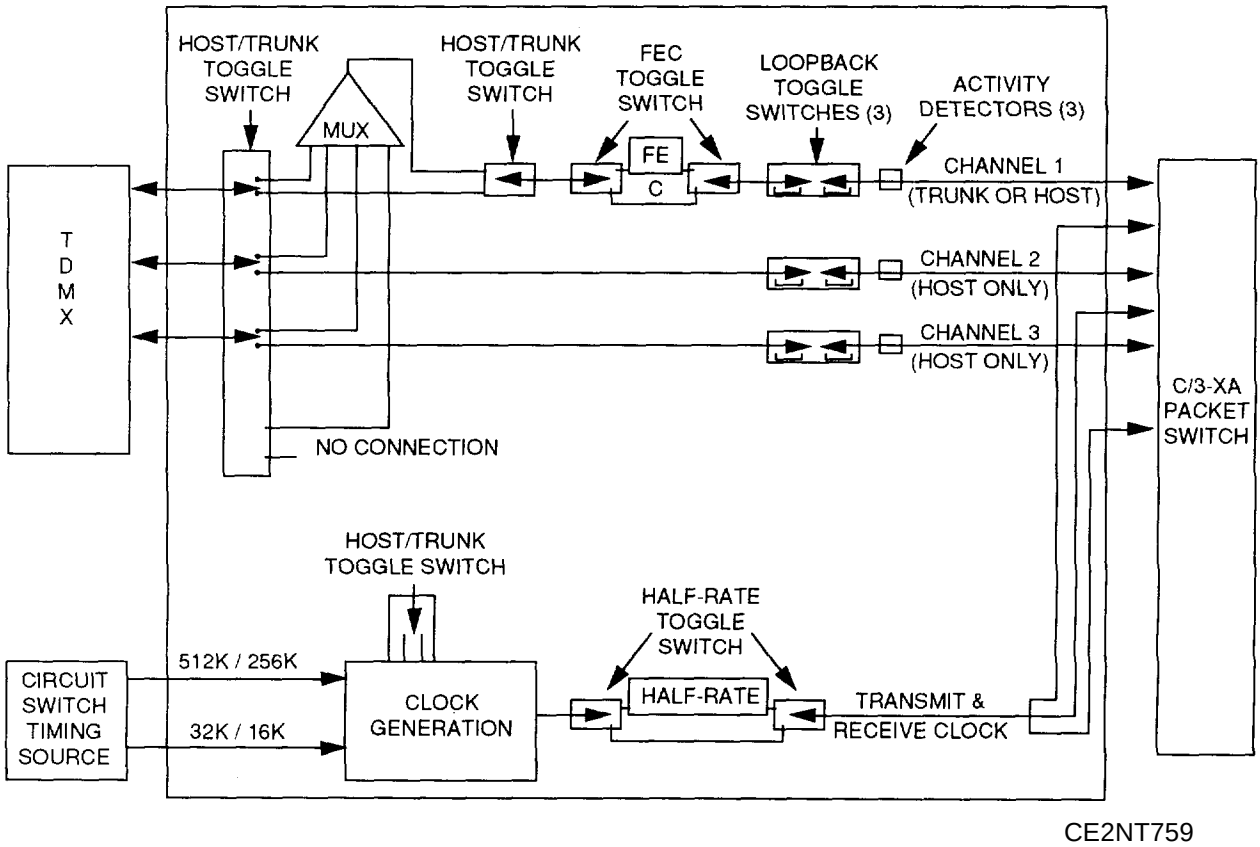

Figure 1-63. PSHTI Functional Block Diagram

1-33 PS INTERFACE DESCRIPTION.

Interconnections within the CC are shown in FO-1 (TM 11-5805-786-12-3).

1-34 TDSG INTERFACES.

There are five RS-423A interfaces from the packet switches to the matrix. Three interfaces are low-speed (16 kb/s) host interfaces while the other two are high-speed (64 kb/s) trunk interfaces. Interface to the matrix is through PSHTI cards. The high-speed ports are used to connect the CC packet switch to packet switches in the connected NCS switches over four adjacent channels of the interswitch trunk group. Two low-speed ports are used to connect to the packet switch at the SEN over SEN interswitch trunks. One low-speed port is a dial-up port, which allows a data subscriber to dial into the PS network.

1-35 COMMERCIAL OFFICE INTERFACE.

The CC provides a commercial office interface using dc closure trunks to a TC LTU (DLTU card) on the CV-4180 (dismounted LTU).

1-36 SUPER HIGH FREQUENCY AND VERY HIGH FREQUENCY RADIOS.

1-36.1 Super High Frequency (SHF) Radios. The SHF radio kits provide a backup means of access to an adjacent CC, LEN, NCS, or LOS assemblage when cable access is not practical. The Optional SHF radio kits are used in NCS, LOS (V) 3, LOS (V) 1, and SEN assemblages, and the fixed SHF radios are used in LEN and LOS (V) 4 assemblages. On the CC, the controller is set up outside the shelter and is interfaced through a connector on the SEP.

The SHF radios have an RF interface with each other in two ranges; i.e., 14.648 to 14.816 GHz and 15.033 to 15.201 GHz. If equipped, the radios may operate over the 14.5 to 15.35 GHz range. This interface supports TDM rates of 256, 512, 1024, and 4096 kb/s.

When an SHF radio is used, the modulation is bypassed and the baseband of the multiplexed DTG (DTG 26) is patched into the SHF radio controller.

The SHF radio function (SHF band) uses low power and narrow beams and has inherent anti-jam features.

1-36.2 CC Radio Access Unit (RAU) Functionality. The CC shelter includes four RT-1539 very high frequency (VHF) radios and a group logic unit (GLU). The radios interface to an omnidirectional antenna mounted on a 15-meter or a 30-meter mast. The radios are coupled to the antenna through an RF multicoupler. This enables the CC to interface to mobile subscribers without connecting to a RAU shelter. The CC has half the number of channels available as a RAU.

Mobile subscriber radiotelephone terminals (MSRTs) can download frequency plans from the GLU by connecting to a, connector on the CC SEP.

The CC shelter can also connect via DTG to a RAU shelter, either by direct coaxial connection or via a LOS radio link. The standard CC database has two RAU DTGs in addition to the four internal RAU radios.

CC shelters can operate in MSRT mode when on the move. This is done by setting radio #4 and the RF multicoupler to MSRT mode. The HMMWV battery is used to power the radio. The shelter whip antenna receives and transmits signals, and the subscriber communicates via a DSVT in the cab of the HMMWV.

1-37 NET RADIO INTERFACE.

The MSE System provides an interface to the Combat Net Radio (CNR) at the CC. The CNR is a Government furnished ANNRC-46 or ANNRC-90 single-channel ground airborne radio system (SINCGARS) radio. The radio and its antenna are mounted outside the shelter. The NRI is a half-duplex (push-to-talk) interface.

The CC allows interfacing with the optional CNR via the KY-90. The KY-90 includes COMSEC encryption compatible with DSVTs in the MSE network, therefore, the switch recognizes the KY-90 as a DSVT. The KY-90 uses Vinson encryption to encrypt the radio link.

Radios configured for automatic CNR operation can bypass the KY-90, allowing calls in either direction without manual intervention. The actual hardware interface is identical to the CC in both cases.

1-38 OPERATING SOFTWARE.

1-38.1 General. In any configuration, the circuit switch operating software is capable of performing the functions and providing the services necessary to support circuit switch systems level operations. The operational software functions are organized into independently assembled programs which operate under the control of an executive program. As a real-time system, the circuit switch software is driven by external events. The arrival time of these events into the system may be with variable time distributions. Thus, a basic requirement of the system design is to provide for the servicing of random events occurring at random times with random distributions.

Random arrival queue is an integral part of the software design. Queue servicing is provided by each program module on a FIFO basis. Each queue entry represents a request for a specific service. An externally queued event represents a request for processing to several different circuit switch programs. A given program may, in turn, through the use of subqueues, initiate specific subroutine functions.

The main program flow determines when a requested service has been accomplished. Typically, a response for each specific queue or subqueue entry, which has been serviced, is presented back to the specific program that requested the queuing for service. Thus, a basic three-stage process exists for servicing typical random events, namely, queuing for service, processing the queue, and returning a response to the program that requested the service that the service has been completed. All queues are serviced promptly.

All programs are processed according to all their applicable queues, and other inputs when they are initiated. This action ensures a minimum accumulation of queue entries. Consequently, there is, even in a peak-bad period, virtually no accumulation of backlog work to be accomplished by any program at any one time. Each major program is defined, organized, and structured according to a strict delineation of the functions it is to provide for the system. Although there is a high level of intercommunication and system interdependence among the various major programs, the individual programs are each functionally and structurally modular.

The overall control of the circuit switch software system includes both hardware features of the circuit switch processor and the operating system software.

An outline of the circuit switch operating software features is provided below:

- The operating system schedules the major programs, services interrupts, and initiates program activity
- The I/O programs, within the operating system, take care of real-time hardware-generated inputs and outputs, and the operator/machine I/O interfaces
- The scanning program processes scanner hardware-generated inputs
- The signaling program processes the real-time receiver inputs (incoming signaling) and performs outgoing signaling
- The digit analysis program processes access codes and telephone numbers and applies call restriction criteria
- The routing and matrix management program selects, reserves, and bookkeeps the circuit switch matrix paths and associated pooled equipment and also maintains a record of the connections and equipment that are in use

- The common channel signaling programs process signaling messages sent to and received from other circuit and message switches through the trunk signaling buffers
- The call extension programs provide for the control of outgoing signaling and supervision sequences
- The traffic service attendant position program provides for operator-maintainer service processing
- The operator/machine program processes the data associated with the workstation visual display, digital computer, keyboard, printer, floppy drive, and system alarm panel operations. It also supports the on-line fault detection software
- The on-line fault detection program is responsible for the operator-maintainer initiated testing of the system's hardware
- The flood search routing function (FSRF) software is responsible for locating paths to called subscribers or gateways for call routing
- The start-up/recovery programs provide the initialization of both the database and the external devices following start-up or switchover

Thus, the overall control of the circuit switch is attained by the orderly interaction of the switching hardware, the circuit switch processor, and the operational software

1-38.2 Program Levels. Program levels are determined by the analysis of the order in which the programs should run. The central processor has a hardware mechanism called the auction. The auction is a computer logic sequence that inspects the status and enable bits associated with each program level. There is an ordered set of 64 pairs of bits, one for each program level. These bits reside in the CPU's base memory, page zero. When an auction occurs, the first pair of status/enable bits that are both set to one cause the CPU to transfer processing control to the corresponding level where processing continues.

Typically, after the execution of a program level, the software at that level turns off its own status bit, thereby allowing the auction to select the next program to run that has both status/enable bits on.

1-38.3 Interrupts. There are 18 interrupts that are utilized by the system. These interrupts are serviced as three different priority groups: high priority, medium priority, and low priority. High priority interrupts are handled by I/O handler #1, medium priority interrupts by I/O handler #2, and low priority interrupts by I/O handler #3.

1-38.4 I/O Request. The circuit switch operating software services all I/O requests. The I/O software consists of logical I/O and physical I/O programs. The logical I/O is the software that interfaces the application programs and the hardware. The logical I/O services the application program I/O requests by mapping the request to the physical I/O instructions required to handle the hardware controllers/devices. Changes to the hardware devices do not impact the application programs. The physical I/O directly services the I/O operation and, upon completion, returns status of the result to the application program.

1-38.5 Scheduler Function. The circuit switch operating system scheduler schedules all the application programs in a fixed priority sequence at the start of every major cycle. Each application program module, once execution has started, continues to run until it has completed its tasks. Upon completion, the module turns itself off or a 10-ms interrupt occurs. Immediately after the application program module turns itself off, the next highest priority application program automatically starts executing. If a new major cycle starts (100-ms interrupt occurs), the application program will interrupt and effectively be placed on hold until the cycle is completed. Upon return, the application program starts at the instruction location where it was interrupted when its priority level is again activated.

There is one exception to the above that runs in a closed loop: the on-line maintenance program module at the lowest priority in the major cycle. If it has completed all its tasks, it will begin its test sequence all over again. In other words, when the on-line maintenance program module is executing, it will only be stopped by a 1 00-ms interrupt. While the major cycle is running, there are other events taking place such as I/O interrupts. If any of these interrupts cause a higher priority level to be activated, the major cycle is interrupted while the higher priority level processing is done. At the conclusion of the higher priority level processing, the major cycle is resumed at the point it was interrupted.

1-38.6 On-line Control and Operational Program. The on-line control and operation program (OLCOP) is the primary on-line software operating system for the circuit switch. Its primary functions are call processing maintenance and traffic control.

1-38.7 Flood Search Routing Function. The FSRF software maintains a database of affiliated, preaffiliated, and duplicated subscribers in the MSE area. The FSRF software communicates with adjacent switches FSRF software to route calls.

1-38.8 Diagnostic. Circuit switch software diagnostics may be run in an on-line or off-line configuration, and may be operator-initiated or run on a continuous basis.

1-38.9 Start-Up. System start-up (cold start) is an initialization process that brings the system to a standby state. The operator-maintainer initiates the start-up process by an AOD command which reads the file from the workstation load disk. The bootstrap loader which occupies the first block on the operational program file, is automatically read into level 63 and control is transferred to the first location in level 63. The level 63 program then reads the start-up program module into memory and transfers control to it. The start-up program module then goes into a system initialization process consisting of:

- Loading the system operational program
- Initializing each device with a reset command
- Initializing the system I/O buffer control tables for use by the operational program
- Accepting as an input parameters time-of-day and switch type from the ASI command
- Loading database from the workstation load disk via AOD command
- Push button to go active
- Reading the CAP/CEM to create the system configuration map
- Start sending the standby keep-alive signals
- Sending a message to the operator/maintainer on the VDT that start-up processing has been completed.

1-38.10 CAP/CEM Monitoring. During each major cycle, the circuit switch operating system reads the CAP/CEM to determine if the system configuration has changed. It does this by comparing the current CAP/CEM configuration with the status configuration map that it had from the previous cycle. If a change in configuration has occurred, the appropriate program module required to process the change is notified.

1-39 INPUT/OUTPUT SOFTWARE.

The I/O software for the circuit switch operational program is designed to make maximum use of the hardware capabilities of the circuit switch central processor. To accomplish this, it is necessary to have all the I/O software centralized in one package. It is the responsibility of this I/O package to receive I/O requests from the application programs, generate the necessary I/O commands, and service interrupts from the hardware. This process can be divided into two major functional areas: logical I/O and physical I/O (fig. 1-64).

1-39.1 Logical I/O. Logical I/O is the function performed by the application programs to communicate with the I/O package. All communication between the application programs and the I/O package is done through the common database. Logical I/O is divided into two categories: input and output.

Data from input devices is immediately available for processing by the application programs. The data is found in the common database.

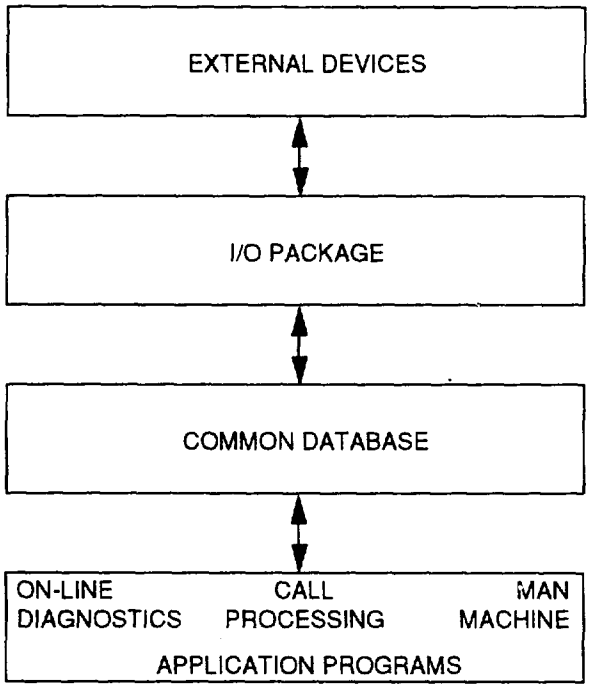

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Figure 1-64. I/O Software

Any application program which has data to output to an I/O device can make an I/O request. I/O requests are made by the application program first running the data in the preassigned fixed length buffer in the common database and then queuing a request to the I/O package. All requests are serviced on the basis of the priority of the device. When the command has been completed, the request is dequeued. The result (successful or unsuccessful) is reported to the application program.

1-39.2 Physical I/O. Unlike the logical I/O, the physical I/O is absolutely dependent on the characteristics of the computer.

Two classes of operation are used to enable the computer to provide control for the execution of data communication with peripheral devices. The classes are programmed input/output and automatic input/output. Programmed input/output is computer instruction-dependent and the timing is independent of the peripheral device. Programmed I/O has a limited amount of use by the I/O package and is used mostly for maintenance and diagnostic purposes. Automatic I/O is independent of instruction execution and takes place at the peripheral device rate. Automatic I/O is controlled by special control words (keyword and termination word).

The keyword contains the mode of operation, the block length, and the data address in memory; it is used during each data word transmission. The transmission word is used at the end of a block of transferred data by device interrupt or upon fault detection. It is used to specify status and program level to be activated at the completion of the I/O operation. Automatic communications are initiated by programmed instructions. Prior to automatic I/O, the control words must be initialized. Automatic I/O is the mode of operation used most frequently.

1-39.3 I/O Handlers. The workload for the I/O package has been divided between three independent program levels: I/O handlers 1, 2, and 3. This division is made to allow the I/O to service the devices on a priority basis. I/O handler 1 services interrupts only, I/O handlers 2 and 3 service interrupts and application requests.

1-39.4 I/O (Control) Devices. The following paragraphs describe the I/O devices in terms of their basic characteristics as seen by the circuit switch software (fig. 1-65).

1-39.4.1 Workstation VDT. The switching processor software interfaces the workstation via the VDT controller. The VDT uses standard ASCII code. The VDT is capable of displaying 25 lines of 80 characters. Three lines are reserved for data readout (protected) from the processor. This data cannot be changed through the keyboard. The remaining lines of data will be either computer-initiated or keyboard composed. The VDT contains a refresh memory, capable of storing 2000 ASCII characters.

1-39.4.2 Workstation TTY/CSP. The WS uses the TTY controller interface for TTY, and the CSP emulation mode. Also, the TTY/CSP uses standard ASCII codes of seven data bits and one parity bit. Keyboard entries are sent to the processor in a byte-input mode. Up to 2048 bytes may be sent in the automatic output mode to the controller. The TTY controller will go to the quiescent mode at the conclusion of either input or output mode.

1-39.4.3 Load Disk. The switching processor transfers files to and from the workstation load disk using the IOSL controller which interfaces to the small computer system interface (SCSI) bus.

1-39.4.4 Switching Controller Group. The SCG is a centralized group of controllers dedicated to the circuit switch switching equipment such as scanner, senders, receivers, special devices, and matrices as well as servicing the fault and test function. Data is transferred to and from the processor and the switching equipment. All commands to these switching devices must pass through the SCG. The effect of the SCG is essentially transparent to the operational software except for the diagnostic program.

1-39.4.5 Signaling Buffer. The SBC performs the function of routing messages and commands between the processor and the TSBs and the DIBTS buffer.

1-39.4.6 COMSEC. The COMSEC controller is part of the COMSEC control link between the CPU and the COMSEC communications equipment facility.

1-40 DATABASE ORGANIZATION.

The circuit switch operating software is a table driver system. Data is collected in information tables which depict physical representations of the hardware, status conditions, or processes. This collection of information tables is referred to as the database. The logical organization of the database is aimed at structuring information in a form that allows for efficient operation of the computer programs and ensures that the operation software can maintain control of the system. The circuit switch data tables contain all of the necessary information that is used by the circuit switch software to:

- Keep track of system hardware usage
- Manage the processing sequences for the loops and trunks
- Maintain a dynamic record of all status, conditions, and classmarks
- Perform routing control, subscriber service control, cryptographic control, call restriction control, digit editing and translation, incoming and outgoing in-band and out-of-band signaling and supervision
- Provide for call service position and switch supervisory operational functions
- Evaluate system hardware conditions
- Control software operating sequence and timing
- Communicate to and from the hardware
- Perform interprogram communication and control
- Record the configuration of the switching system. Provide statistics on the dynamic operation of the system.

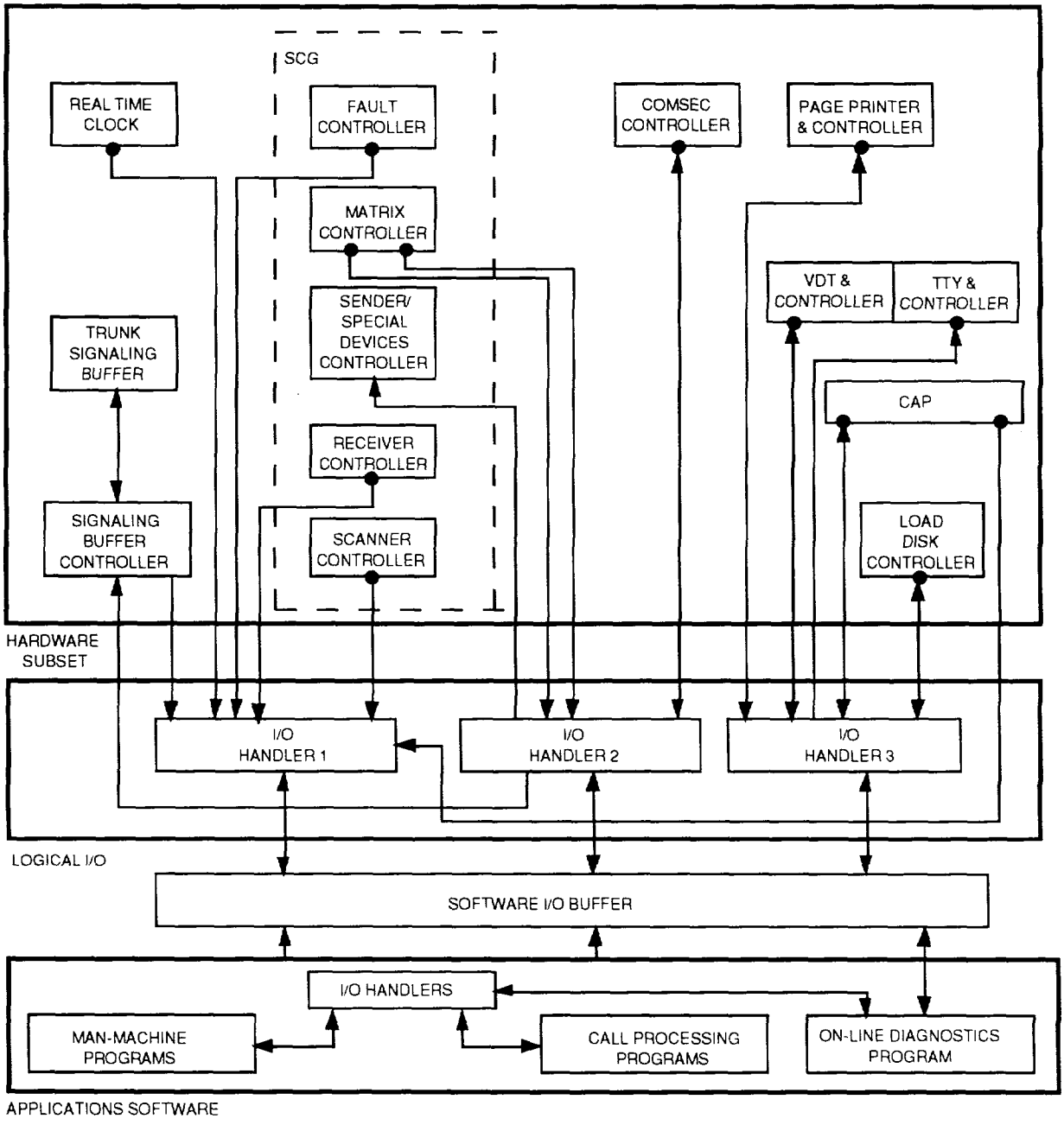


Figure 1-65. Software View of Hardware, Block Diagram

1-41 CIRCUIT SWITCH ON-LINE CONTROL AND OPERATIONAL PROGRAM (OLCOP).

1-41.1 General. To permit external event interrupt processing, OLCOP operates on a major/minor cycle time base. Those programs that are to be serviced every 100 ms are run every major cycle. Likewise, those programs which must be run on a shorter time base are run every minor cycle (20 ms) (fig. 1-66).

When OLCOP is executing any program, an external or timing interrupt may occur. The hardware function of the circuit switch processor immediately causes the executive-interrupt handlers to service the interrupt. The interrupt servicing is provided on the basis of the interrupt priority. Examples of high priority interrupts are scanning inputs, receiving inputs, and trunk signaling channel inputs.

These interrupts occur relatively infrequently and require little processing but must be serviced quickly. All interrupt service requests for relatively slow operations, such as VDT inputs from the operator-maintainer's position or outputs from the processor to the VDT, take a low priority order; they are serviced after those functions requiring a higher priority of service. The interprocessor communication program, ECOM, uses the processor-to-processor interface (PPI) function to transfer the necessary data needed by the standby processor to carry on all processing in the event of a processor switchover.

The power-on and start-up programs perform the initial processing necessary to start the operational software from a cold load start.

The error control level (ERRR) comprises those functions needed to service conditions, detected by the CPU, that indicate a software or hardware error. Most of the conditions resulting in the passing of control to ERRR result in the processor switchover. The recovery program performs the start-up of the standby CPU when it is in transition to become the active CPU. The recovery program also acts to maintain the existing calls during switchover.

1-41.2 Call Processing Function.

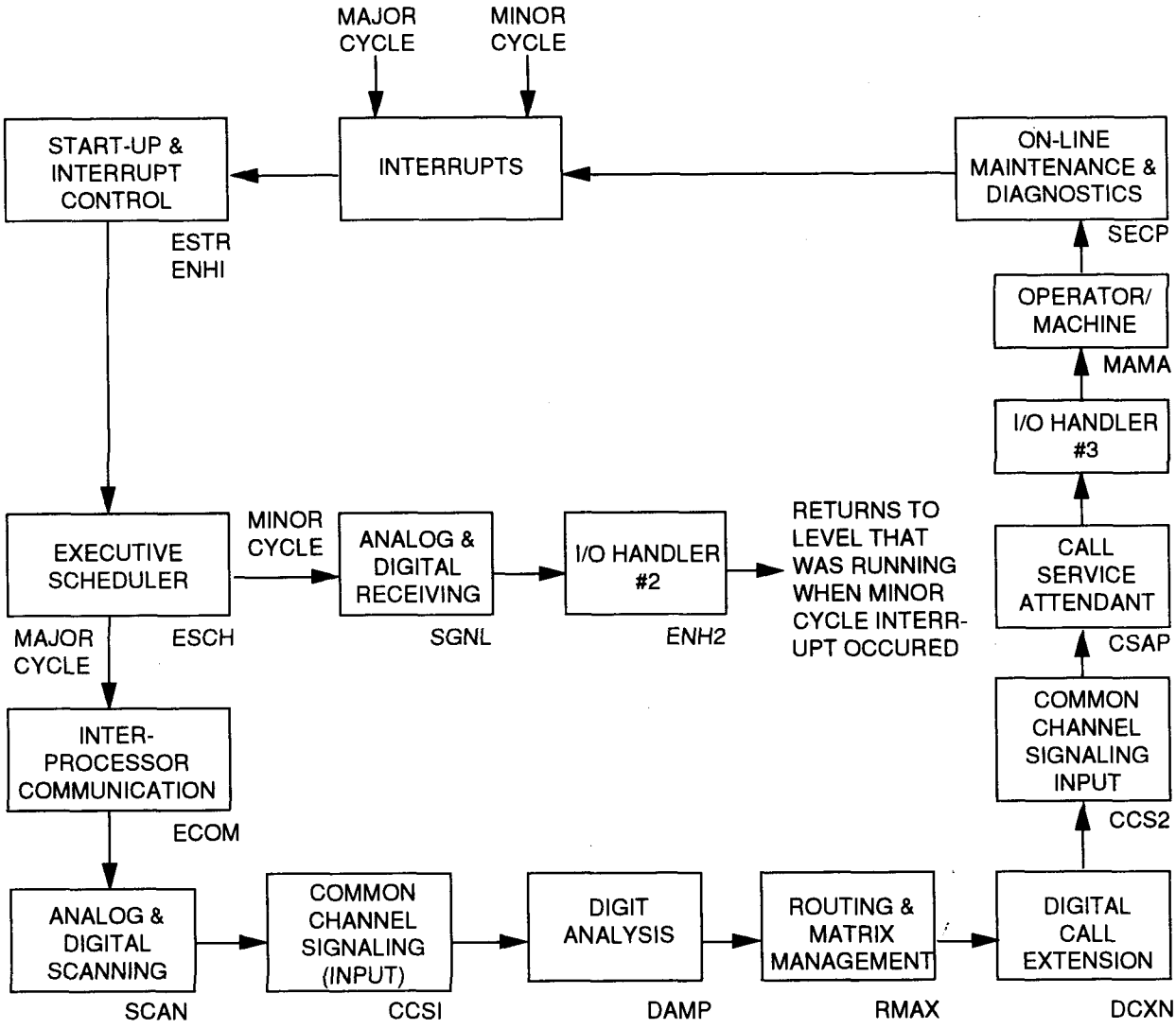
1-41.2.1 Scanning Program. The primary purpose of the scanning (SCAN) program is to process the inputs from the cyclic scanner input buffer. This processing includes the validation and initial interpretation of ac, dc, and digital scanner inputs; and timing the input sequences as required. The program also determines changes in the state of the line; for example, on-hook to or from off-hook. Scanning receives dial pulse digits from the dc scanner and manages its own timers for terminal supervision.

Scanning (SCAN) is operated once every major cycle and processes all available new inputs from the scanner buffer. All valid scanner inputs that represent a change-of-state for terminal supervision result in outputs from scanning to one of the other call processing programs. Scanning performs the necessary metering of traffic statistics for the traffic metering function. SCAN sends work to SGNL for sender and receiver operations and to RMAX for party path connections.

1-41.2.2 Signaling Program. The primary purpose of the signaling (SGNL) program is to process the inputs from the cyclic receiver input buffer. It also processes the requests from other programs for controlled invocation of senders, tone busses, echo suppressers, and LTU signals that require (20 ms) granularity timing. The digital .receiver inputs, after being validated by signaling (SGNL), are forwarded to digital call processing. Each valid digit is saved in the call register table for later analysis by the digit analysis program (DAMP).

SGNL is one of the minor cycle programs that is initiated every 20 ms by the executive. SGNL manages a termination status, accounting, and timing for the various tone signaling devices. SGNL handles requests for processing from DAMP to suspend digit reception when a conference dial tone is needed. It also services requests from the on-line fault programs for initiating test tones.

1-41.2.3 Digit Analysis Program. The primary purpose of the DAMP is to analyze and translate an incoming string of characters and digits which have been received at the circuit switch from subscriber loops or from a switch trunk. A secondary purpose of DAMP is to service task requests received from other call processing programs. Typically, access codes precede a telephone number. DAMP interprets the access codes (if any) to determine which special services are desired by the calling party. The DAMP program also translates the called telephone number to determine which circuit terminal(s) may be used to extend the call.



PROGRAM MODULES RUN IN SEQUENCE UNTIL:

A. ALL WORK HAS BEEN PROCESSED OR
B. AN INTERRUPT OCCURS

Figure 1-66. On-line Control and Operational Program Flow Diagram

DAMP looks at each call register that has the new input digit(s), processes any new input and, when all the needed digits have been received and analyzed, marks that call register for subsequent processing by RMAX. DAMPs secondary purpose is to service processing requests from other call processing programs. Many of the stimuli for these requests come initially from DAMP through other call processing program levels and back to DAMP. When DAMP sends requests to other call programs, it will not continue processing the call register until a reply to its request is received.

The call register is the main data table used by DAMP. DAMP analyzes the digit strings in the call register. When it has completed the analysis of the first digit of the string, DAMP sends a route pointer through the call register to RMAX. The pointer indicates that's a loop, a trunk group, or a line hunting group is to be used to call the desired party. A deterministic route is usually not assigned to the LEN circuit switch. When DAMP does not find a route to the called subscriber, it requests a search by the routing processor.

1-41.2.4 Routing-Matrix Management. The primary purpose of routing-matrix management (RMAX) is to manage the physical equipment resources of the circuit switch. In routing a call, RMAX uses the route pointer provided by DAMP to select a local line hunting group, a local loop, or a trunk. RMAX selects the common equipment that is needed to complete the call.

The management routines include matrix paths, key changes, and trunks. These routines issue commands to connect and disconnect the matrix paths and busses, and later process the status of these commands to ensure proper operations. The RMAX processing is initiated by requests sent to RMAX from the other operational programs.

The application of pre-emption against all resources used in existing calls of lower precedence is performed by RMAX. RMAX selects conference bridges and connects and disconnects conferees. It also manages the traffic service attendant bridge(s). In performing these major functions, RMAX maintains database tables that contain the maps of the connections that are in use and/or reserved for use.

1-41.2.5 Digital Call Processing. The primary purpose of digital call processing (DCXN) is to perform most of the processing for digital subscribers and analog subscribers terminated on the TDMX through DLTUs. Digital scanner inputs are, after being parity-checked by SCAN, forwarded to DCXN for analysis and digital application. Digital receiver inputs are parity-checked by SGNL and forwarded to DCXN for analysis and digital application.

The common channel signaling programs set up work for DCXN when TDMX terminations are involved in digital trucking operations. DCXN manages the DSG utilization and controls the COMSEC CEF and TED operations. The logic for COMSEC stage I and COMSEC stage II call control constitutes the largest portion of the DCXN program.

1-41.2.6 Common Channel Signaling Programs. The primary purpose of the common channel signaling programs (CCS 1 and 2) is to provide the processing necessary to manage the out-of-band (OOB) signaling and supervision of calls between one circuit switch and other circuit or message switches. CCS 1 initiates through DCXN connections and disconnections of matrix through-paths for call answer, or call release messages. Test sync and trunk test messages are used by CCS 1 to initiate common-channel-character-sync verification and to service the on-line fault detection processing, respectively.

Routing (RMAX) and the digital call processing (DCXN) programs provide CCS 2 with request for service. CCS 2 functions to generate the common channel signaling messages appropriate to the Call State.

The primary purpose of the call service attendant processing (CSAP) program is to allow one or more operator maintainers to provide assistance to subscribers. CSAP processes all operator-maintainer's control panel requests by interpreting and analyzing the operator-maintainer's digital receiver inputs forwarded by SGNL to CSAP. The CSAP program also keeps a record of which operator-maintainer station is staffed or not staffed.

The management of the operator-maintainer 2-port bridge is the responsibility of CSAP for all SPLIT, HOLD, and RELEASE actions. The call processing programs regard the operator as wholly privileged to invoke any service available through the console. The CSAP program generates its own TDMX connect/disconnect commands and verifies the matrix status returned, all through the I/O software. Control of lamps and alarms on the operator-maintainer's console is performed by CSAP prompting signals from the DSG to the operator-maintainer's signaling port.

1-41.2.7 Operator/Machine Program. The primary purpose of the operator/machine program is two-fold. It first provides the processing necessary to allow the operator-maintainer to enter the system database tables. and to request and receive VDT displays of the condition, status, and configuration of the system. A secondary purpose of the program software is to allow the switch supervisor to initiate any of the on-line fault detection tests. Validation is the process of the program software to verify the structural and syntactical content of an input. Any input which is unidentifiable as to input type or message type, in an improper format, or has data that is unintelligible in content or has values that are not within a pre-defined range, is withheld from the validation tests. A second form of input verification is termed ramification processing. This processing is a specifically bounded set of defined tests employed by the program.

These tests provide to the SSF the basic information on what logical consequences will result if a specific database alteration is executed. The SSF has the option to approve or revoke the execution beforehand.

When the SSF requests an interactive display, the operator/machine program will provide the appropriate VDT screen image. The information displays are populated with the database information by this program as whole screen images in memory. The program then requests I/O service to output the display. Data assignment displays are screen images which, when displayed, allow the operator-maintainer to fill in the open spaces with new data for the use of the software. All system control parameters, classmarks, and timers can be altered in this manner.

1-41.2.8 On-line Fault Detection Program. The primary purpose of the on-line fault detection (ONLFD) program is to detect and analyze all discernible hardware error conditions that may affect the operation of the switching system. The various tests are initiated at different intervals by the system evaluation and control logic in ONLFD.

The call processing programs operator/machine and the executive,. provide services for ONLFD using SGNL, RMAX, DCSN, and the operator/machine program to perform the total software system functions associated with ONLFD. ONLFD tests are initiated when a fault condition is reported over the fault multiplexer, or when a specific anomalous condition is found by one of the other operational programs. All errors or problem conditions discovered by other operational programs are reported to the ONLFD program.

1-42 DIAGNOSTICS.

1-42.1 Software Maintenance. Diagnostics may be performed on the circuit switch equipment while in the online, standby, and off-line modes. Automatic fault detection is accomplished by periodic software test routines and monitoring of hardware fault and status lines. Fault and status reports are provided from the BIT equipment automatically when a fault has been detected, or in response to stimuli from the operational (ONLFD) or off-line maintenance and diagnostic program.

Every fault and abnormal status response is logged on WS TTY log and output to the printer. The printout indicates: the nature of the fault, other equipment utilized in performing the test if software generated, where identification of equipment would aid in the task of fault isolation, and the time to the nearest minute (Julian date) of when the fault occurred. In addition to logging faults, a summary indication is provided to the VDT and the control alarm panel.

1-42.2 Circuit Switch Testing. A description of circuit switch testing is listed below.

1-42.2.1 Test Hierarchy. Circuit switch testing must be performed to ensure an operable system of high availability. The top level consists of some basic integrity tests that are built into the central processor. These are hardware-only tests that must succeed if software is to be loaded into the processor. These tests are automatically performed when the CPU is brought up for operations.

The second level of tests are the off-line CPG tests. All equipment covered by these tests must be up and available if the system is to be brought to a start. The third level has degrees of dependency for on-line and standby test processing. To be able to get at the lower level tested equipment, it is necessary to have passed all of the above tests. The ONLFD programs are logically arranged to play a supporting role in this testing structure. Some of the testing performed by a particular test is not intended to run in the standby computer. Refer to Chapter 3 (Vol. II) for a list of circuit switch ONLFD and periodic tests.

1-42.2.2 Fault Detection by Chaining. Testing is performed and results reported by means of or through a number of individual hardware elements so that a reported fault may be the result of a failure in any one of the elements in the chain. Reported fault conditions can be the result of failure conditions within the functional hardware elements or within the BITE monitoring those elements. Thus, reported faults may not affect traffic handling functions but, if they do, continued use of the failed element may result in further system degradation. Therefore, when a fault is detected, the item being tested will be marked out-of-service if it can be ascertained with reasonable assurance that it is functionally unavailable. Functionally unavailable means the item in question is not capable of handling traffic regardless of whether it has failed or some other element which controls it or which it reports through has failed.

If a common failure is indicated, testing of the group of items will cease until directed by the operator-maintainer when he commences the fault isolation procedure. A message will be output to the printer and VDT, to indicate that testing of the group of items has been discontinued.

1-42.2.3 Continuous Hardware Monitoring. Continuous hardware monitoring is provided for equipment that:

- Is redundant and switched over by internal BITE due to a time constraint on switchover
- Can, if failed, contribute to violation of COMSEC doctrine, most notably
- Special situations, most notably transmission equipment, where software testing is not feasible.

In the case of hardware-switched redundant items, switchover occurs coincident with reporting of the fault if the standby unit is good. Switchover will not occur to a known defective unit. A fault report does not guarantee that the reporting element may have been the cause. Therefore, further isolation is, in general, necessary.

1-42.2.4 Status Returns During Call Processing. Interaction between call processing software and the hardware performing the specified function will result in the return of status information to software.

Returned status may be as simple as a parity error report from the affected controller or as complicated as diagnostic return from the TDMX. All status returns indicating fault conditions are printed on the printer. Software functions automatically execute the appropriate commands and log the results on the printer.

Software, in general, performs an information gathering function and not a fault isolation function. Only in those cases where a status report indicates a fault relating to a processor/controller interface (such as I/O parity error), the software then automatically performs a fault isolation function to determine whether the controller or processor is at fault, Upon making the determination, software will initiate switchover of the suspected faulty unit.

1-42.2.5 Periodic Testing. Software initiated periodic testing is employed to test various items of common equipment which are not otherwise testable, to test BITE, to perform continuity type checking on trunks, and DSVT loops and to perform miswriting tests on the TDMMs.

All periodic tests will be performed on a non-interfering basis with respect to call processing activities. If the BITE required for a particular test is out-of-service, that test will not be performed.

1-42.2.6 Operator-Maintainer Requested Tests. The operator-maintainer is capable of requesting specific tests to aid in performing fault isolation and is also capable of marking equipment in- and out-of-service. The ability to mark equipment in- and out-of-service is absolute. It is assumed that the operator-maintainer performs adequate testing to validate equipment operability prior to marking it in-service.

Operator-maintainer requested tests are given precedence over periodic testing. Every operator-maintainer requested test receives periodic testing. Every operator-maintainer requested test receives one of the following three indications: equipment busy, equipment good, equipment failed. If failed, an error vector, providing an indication of the nature of the failure by reference to a maintenance manual, may be part of the acknowledgment. All output messages include time-of-day information to the nearest minute.

Equipment busy is indicated if the requested item is in use or reserved or if the test item is pre-empted to completion of the test. The operator-maintainer can, if desired, force a test of a busy equipment item by first marking it out-of-service and then requesting a test. The operator-maintainer is capable of identifying specific common equipment items for use in the test and is capable of requesting through a single command, a test of up to eight units of the same type as long as the units are sequentially numbered.

1-42.2.7 On-line Fault Detection (ONLFD). The on-line fault detection program is part of the on-line control and operational program (OLCOP) and is activated on a time-available basis by the executive scheduler. The ONLFD functions are split between the system evaluation and control program (SECP) and the ONLFD test program units. The system evaluation control program (SECP) exercises overall control of the maintenance and diagnostic tests. SECP is scheduled by the executive scheduler to run each major cycle (100 milliseconds). Each cycle results in execution of one or more of the ECP functions.

SECP controls the execution of individual programmed tests whether the tests are initiated automatically or by an operator-maintainer request. The tests associated with ONLFD are executed for one of three reasons. Certain tests are run on a periodic basis in sequential order. Other tests are run only when a particular type of fault occurs in the system and software is necessary to evaluate the fault.

The last type is tests requiring operator or operator-maintainer interaction and are run only when requested. These periodic tests may also be requested for execution out-of-sequence by the operator-maintainer.

1-43 TIMING CIRCUITS.

The timing circuits provide all clock signals required to operate the circuit switch (refer to FO-2). They consist of a MTG, three LTGs and a timing generator, all of which are redundant. The MTG generates four basic timing signals which are derived from a precision crystal oscillator located in the MTG oscillator assembly which is phase-locked to a more accurate source.

The timing signals are slaved to the frequency reference oscillator (FRO) or to one of four recovered clocks from predetermined DTGs (DTGs 1, 2, 16, or 17). In the event of a degradation or failure in the primary MTG, the backup MTG is used to maintain clock frequency continuity. Card locations are given for both primary and secondary Mtgs. and LTGs.

Normally, timing will be derived from the FRO. If the FRO is not available, the output of the MTG is forwarded to LTGs. They derive all the clocks required by the circuit switch from the five basic frequency timing inputs. The timing generator generates all the low frequency clocks required by the switching equipment from the output to the LTG. It is located in the CEG.

The recovered clock selection is manually controlled and based on the highest quality level (lowest bit error rate) of recovered clocks from the four collectable group modems. Since this signal may be one of several frequencies, the CPG reports the framing channel bit error rate of all transmission groups. The transmission group recovered clock is selected at the recovered clock panel.

For proper recovered clock acquisition, the SYNC SOURCE selector switch (located on the CEG patch and control panel) must be positioned to MASTER for FRO source or position 1, 2, 3, or 4 for DTG selection. For position 1, 2, 3, or 4, the group rate selector switch must be set to the appropriate transmission group frequency.

The MTG consists of six modules and two precision voltage control oscillators (MTG oscillator assemblies). The controller circuit together with the MTG oscillator assembly generate 12.288 MHz square waves which are forwarded to the synthesizer circuits. The synthesizer circuits generate 18.432 MHz, 16.384 MHz square waves, and 100 Hz sync pulses from the 12.288-MHz input. These frequencies along with the 12.288 MHz are distributed through digital line drivers (distributor drivers), to LTGs located in the user rack. The primary MTG (phase-locked to the FRO reference) is used as a prime frequency source during normal operation.

The backup MTG is available in the event a failure or degradation occurs. The primary and backup Mtgs. are precision voltage controlled quartz crystal oscillators which are slaved to the recovered clock, and are capable of stand-alone operation in the event the recovered clock is not available.

The LTGs provide the required output clock frequencies for circuit switch operation. The output clocks are derived from the 12.288-MHz, 16.384-MHz. and 18.432-MHz inputs from the MTG. The 1 00-Hz sync input is used to synchronize the LTGs. All LTGs are redundant, with selection of the primary or secondary LTG controlled internally or by manual front panel control.

The digital switching equipment contains two LTGs, one designated red, the other designated black. The red LTG provides a clock frequency for unencrypted secure call processing. The black clock frequencies are used for encrypted or non-secure call processing. Using separate LTGs provides isolation between secure and unencrypted non-secure call processing. This provides additional security.

The timing generator is used to derive low frequency timing signals by counting down from a 4-kHz clock provided by the LTG. The timing generator provides timing signals for the switching equipment. These low frequencies are primarily employed for on/off tone gating.

1-43.1 Automatic Switchover of Timing Generator. Automatic switchover from the primary MTG to the backup MTG occurs under either of the following conditions (fig. 1-67).

- The fault detection circuits in the distribution driver card detect a frequency fault
- The out-of-sync alarm circuit in the controller card detects a disorder of the control voltage to the MTG oscillator assembly. All faults are reported to the CPG through the special devices controller. When switchover occurs, the distribution drivers are not affected, since the outputs of both synthesizer cards are sent to both distribution driver circuits. Switchover only affects the controller and synthesizer circuits. Switchover of the MTG has no effect in the LTGs which are controlled independently. Therefore, when a switchover from the primary MTG to the backup MTG occurs, the output of the backup synthesizer is sent to the primary LTG through the primary distribution driver. When the MTG fault is repaired, switchover to the primary MTG is initiated by the operator/maintainer through the VDT keyboard.

Automatic switchover from the primary LTG to the backup (redundant) LTG occurs when a fault is detected in the LTG. Under LTG switchover, the LTG receives its inputs from the backup MTG distribution driver. The primary LTG receives its inputs from the primary MTG distribution driver. The outputs of the primary and backup LTG are ORed; thus the recipients of the output clocks are not affected. When a primary LTG fault is repaired, automatic switchover back to the primary LTG occurs.

In order to prevent disruption of the timing circuits when a distribution driver card has to be replaced, all primary LTGs can be manually switched to the backup LTG. This option is provided by the DRIVER A/DRIVER B toggle switch located on the CEG control panel.

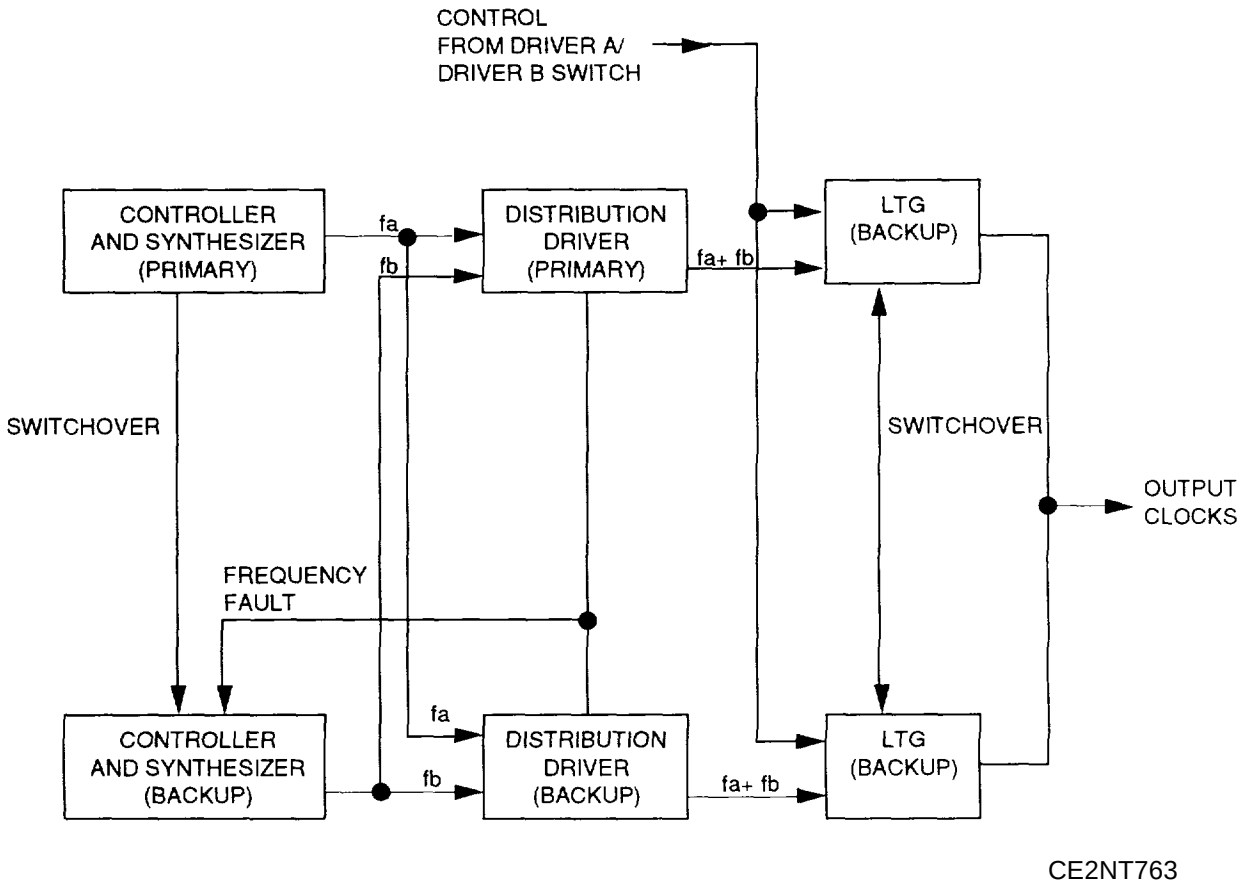


Figure 1-67. Timing Circuits Switchover Block Diagram

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THE METRIC SYSTEM AND EQUIVALENTS

'NEAR MEASURE

. Centimeter = 10 Millimeters = 0.01 Meters = 0.3937 Inches
1 Meter = 100 Centimeters = 1000 Millimeters = 39.37 Inches
1 Kilometer = 1000 Meters = 0.621 Miles

'VEIGHTS

Gram = 0.001 Kilograms = 1000 Milligrams = 0.035 Ounces
1 Kilogram = 1000 Grams = 2.2 lb.
1 Metric Ton = 1000 Kilograms = 1 Megagram = 1.1 Short Tons

LIQUID MEASURE

1 Milliliter = 0.001 Liters = 0.0338 Fluid Ounces
1 Liter = 1000 Milliliters = 33.82 Fluid Ounces

SQUARE MEASURE

1 Sq. Centimeter = 100 Sq. Millimeters = 0.155 Sq. Inches
1 Sq. Meter = 10,000 Sq. Centimeters = 10.76 Sq. Feet
1 Sq. Kilometer = 1,000,000 Sq. Meters = 0.386 Sq. Miles

CUBIC MEASURE

1 Cu. Centimeter = 1000 Cu. Millimeters = 0.06 Cu. Inches
1 Cu. Meter = 1,000,000 Cu. Centimeters = 35.31 Cu. Feet

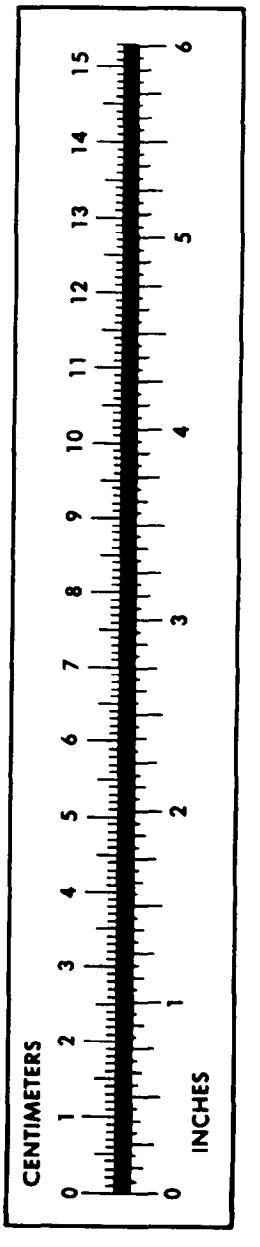
TEMPERATURE

5/9(°F - 32) = °C
212° Fahrenheit is evuivalent to 100° Celsius
90° Fahrenheit is equivalent to 32.2° Celsius
32° Fahrenheit is equivalent to 0° Celsius
9/5C° + 32 =°F

APPROXIMATE CONVERSION FACTORS

TO CHANGE	TO	MULTIPLY BY
Inches	Centimeters	2.540
Feet	Meters	0.305
Yards	Meters	0.914
Miles	Kilometers	1.609
Square Inches	Square Centimeters	6.451
Square Feet	Square Meters	0.093
Square Yards	Square Meters	0.836
Square Miles	Square Kilometers	2.590
Acres	Square Hectometers	0.405
Cubic Feet	Cubic Meters	0.028
Cubic Yards	Cubic Meters	0.765
Fluid Ounces	Milliliters	29.573
ıts	Liters	0.473
arts	Liters	0.946
allons	Liters	3.785
Ounces	Grams	28.349
Pounds	Kilograms	0.454
Short Tons	Metric Tons	0.907
Pound-Feet	Newton-Meters	1.356
Pounds per Square Inch	Kilopascals	6.895
Miles per Gallon	Kilometers per Liter	0.425
Miles per Hour	Kilometers per Hour	1.609

TO CHANGE	TO	MULTIPLY BY
Centimeters	Inches	0.394
Meters	Feet	3.280
Meters	Yards	1.094
Kilometers	Miles	0.621
Square Centimeters	Square Inches	0.155
Square Meters	Square Feet	10.764
Square Meters	Square Yards	1.196
Square Kilometers	Square Miles	0.386
Square Hectometers	Acres	2.471
Cubic Meters	Cubic Feet	35.315
Cubic Meters	Cubic Yards	1.308
Milliliters	Fluid Ounces	0.034
Liters	Pints	2.113
Liters	Quarts	1.057
ers	Gallons	0.264
ms	Ounces	0.035
ograms	Pounds	2.205
Metric Tons	Short Tons	1.102
Newton-Meters	Pounds-Feet	0.738
Kilopascals	Pounds per Square Inch	0.145
lometers per Liter	Miles per Gallon	2.354
meters per Hour	Miles per Hour	0.621



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